Residual Stress Distribution in Stacked LSI Chips Mounted by Flip Chip Technology

Nobuki Ueta and Hideo Miura
Fracture and Reliability Research Institute, Graduate School of Engineering, Tohoku University
6-6-11-716 Aoba, Aramaki, Aoba-ku, Sendai, Miyagi 980-8579, Japan
Tel: +81-22-795-4830, Fax: +81-22-795-4311, E-mail: ueta@rift.mech.tohoku.ac.jp

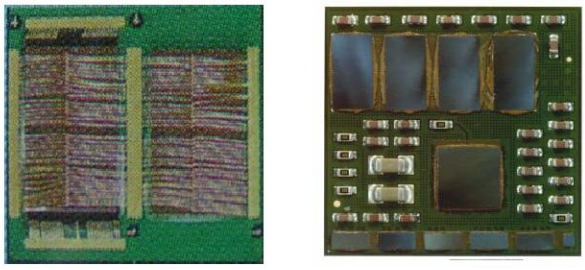
Abstract

Since mechanical stress affects both electronic functions and reliability of LSI chips, it has become strongly important to minimize the residual stress in LSI chips. This is because the residual stress increases significantly by changing the bonding structure between an LSI chip and a substrate from a wire-bonding structure (WB) to a flip-chip structure (FC). A finite element analysis, therefore, was performed to make clear the quantitative residual stress distribution in stacked chips mounted by flip chip technology using area-arrayed metallic bumps. The maximum value of the normal stress on a transistor formation surface of a chip shifts about -200 MPa by changing the assembly structure from WB to FC. A periodic distribution with amplitude of about 90 MPa also appears due to the periodic alignment of the metallic bumps. Such a change of the residual stress in an LSI chip causes a shift of electronic functions of semiconductor devices in a local area of the chip. The important structural factors that determine the distribution of the residual stress are found to be the thickness of a chip, the height of a bump, the width of a bump, the period of the bumps, and the thermal expansion coefficient of underfill material. The average residual stress in the stacked two chips varies depending on the distance from a bending neutral axis of the stacked structure, and the local residual stress also varies depending on the relative position of bumps in an upper connection layer and a bottom connection layer. Therefore, it is very important to optimize the thickness of a chip, the position (layout) of bumps, and other structural factors to minimize not only the average residual stress but also the amplitude of the periodic stress distribution. Finally, the estimated stress distribution was proved in detail by experiments using stress-sensing chips with 10-μm long gauges.

1. Introduction

So far, electronic products such as mobile phones and PCs have been miniaturized continuously and their functions have been improved drastically. Three dimensionally stacked structures such as multi-chip modules and multi-chip packages are indispensable for these products in order to increase the assembly density [1][2]. There are various kinds of structures for the multi chip assembly as shown in Fig. 1. One of the most important applications of the multi chip structures is system in package (SiP) that is composed of the combination of CPU chips and memory chips. On the other hand, the methods of the interconnection between an LSI chip and a substrate or another chip are changing from wire-bonding structure (WB) to a flip-chip structure (FC) for maximizing the interconnection density. Since the total thickness of the stack structure is strictly limited for mobile application, in particular, each chip has been thinned to less than 100 μm to minimize the total thickness of the modules or packages,.

These flip-chip structures using area-arrayed tiny metallic bumps such as Cu or solder are covered insulating material (underfill) such as epoxy or plastic for assuring the reliability of the connection between an LSI chip and a substrate or another chip. Since the mismatch in the material properties such as the coefficient of elasticity and the thermal expansion coefficient between metallic bumps and underfill, the periodic stress distribution appears near the interface between the chip and the bumps layer. The local deformation of the chip caused by thermal stress increases drastically because the bending modulus of the thinned chip decreases significantly. The local residual stress also varies depending on the relative position of bumps in an upper layer and a bottom layer. In addition, the average residual stress in the stacked chip changes depending on the distance from a bending neutral axis of the stacked structure. Such a localized high stress or strain may give rise to fracture such as delamination or cracking of materials [3]. Since high stress and strain deform the crystallographic structure of the materials, the electronic functions and reliability of the chips



(a) Wire-bonding structure (b) Flip chip structure

Figure 1. Multi Chip module structures for system in package.

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may deteriorate due to the change of band gap of semiconductor or dielectric materials [4]-[7]. Therefore, it is very important to understand the dominant structural factors that determine the residual stress distribution in stacked LSI chips for assuring the reliability of modules and packages.

In this paper, the residual stress distribution in the LSI chips stacked by flip-chip technology and the important structural factors that determine the residual stress distribution are analyzed using a finite element method. In the addition, the estimated stress distribution is proved by stress measurement of Si chips mounted by flip-chip technology by using stress sensing chips composed of 168 poly-crystalline-silicon-film gauges of 10-μm in length.

2. Analysis of Residual Stress Distribution Using a Finite Element Method

2.1 Example of Finite Element Model

Figure 2 shows an example of a finite element model for the stress analysis of 2 chip-stacked structure. The width of the substrate was assumed to be 6 mm. The thickness of the substrate is 1 mm. The width and the height of Cu bumps are fixed at 100 μm, respectively and the pitch of the bump is assumed to be 200 μm. Two relative positions of bumps in the upper connection layer and the bottom connection layer are assumed. One is the same bump alignment model (Fig. 2(a)), the bumps in the upper layer exist at the same positions where the bumps in the bottom layer exit. The other model is called the different bump alignment model (Fig. 2(b). In this model, bumps in the upper layer exits at the same position where underfill exists in the bottom layer. Assuming the symmetry of the total structure, the half of the total structure is modeled for the stress analysis. The total number of the nodes of the three dimensional model and elements are 27025 and 26640, respectively. The two-dimensional generalization plane strain model is used in this analysis. The materials constants used in this analysis are summarized in Table 1. Most materials were assumed to be elastic materials. Only Cu is modeled as elastic-plastic material. Yield stress of the Cu is assumed to be 300 MPa. The chip is mounted on an organic printed circuit board at 150℃. The maximum value and the maximum amplitude of the normal stress along x-direction near the interface between the Si chip and the bump layer are used for evaluation parameters of the shift of electronic functions of semiconductor devices.

2.2 Periodic Residual Stress Distribution in the Stacked Chips Mounted Using a Flip Chip Technology with Area-arrayed Metallic Bumps

The distribution of the normal stress along x-direction on the transistor formation surface of the chip mounted by a

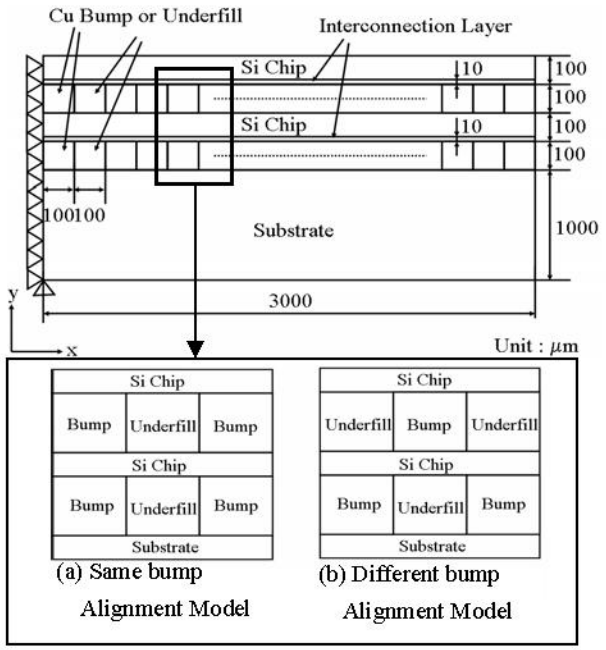

Figure 2. Finite element model for analysis of residual stress in Si chips mounted on a substrate by flip chip technology

Table 1 Materials constant

Material	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (10^{-6}/K)
Si	130	0.28	4.2
Cu bump	130	0.34	16.5
Underfil	3	0.30	70.0
Substrate	20	0.25	16.0

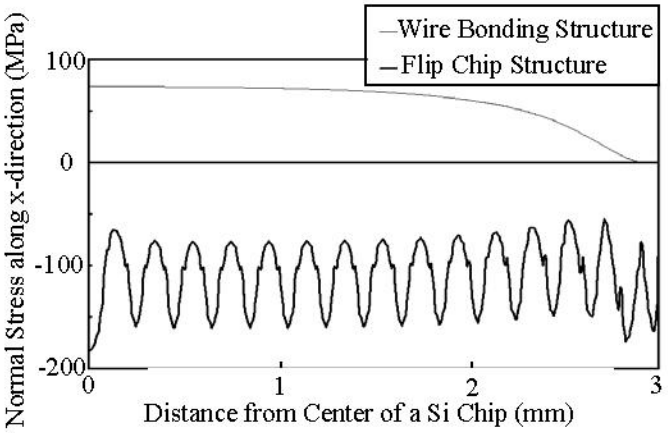

Figure 3. Change of the normal stress along x-direction in a silicon chip depending on assembly structure

wire-bonding structure or a flip-chip structure with area-arrayed metallic bumps is shown in Fig. 3. The width of a chip is assumed to 750 μm. When the chip is mounted using the wire-bonding structure, the residual stress at the interface is almost constant of about 70 MPa, as is also shown in this figure. Therefore, the shift of electronic functions of semiconductor devices is constant in the chip. However, the maximum value of the normal stress on the transistor

formation surface of the chip changes about 200 MPa to the compressive stress side by changing the assembly structure from the wire-bonding structure to the flip-chip structure. A periodic stress distribution also appears due to the periodic alignment of metallic bumps and underfill. In particular, the maximum value of the residual stress is about -160 MPa in the center area of the chip, and the amplitude of the periodic residual stress is about 90 MPa. Such a change of the residual stress in the LSI chip causes not only shift of the average electronic functions of semiconductor devices in the chip but also the local shift of electronic functions of semiconductor devices in the chip. When compressive stress is applied to a PMOS transistor perpendicularly to the channel, its transconductance (Gm) decreases by about 18% per 100 MPa [3]. Based on this reported result, the transconductance (Gm) of a PMOS transistor can be changed by about 16% due to the change of the bonding structure.

2.3 Effect of the Thickness of a Si Chip on Residual Stress

Figure 4 summarizes the effect of the thickness of the chip on the normal stress along x-direction at an interface between the chip and the bump connection layer. In this analysis, the width and the height of Cu bumps are fixed at 100 μm and the pitch of the bump is assumed to 200 μm. The residual stress on a chip surface of a wire-bonding structure is also shown in the figure. When the chip mounted using a wire-bonding method is thicker than 300 μm, the maximum value of the residual stress in the chip is tensile stress of about 50 MPa. But, it is changed to compressive stress when the thickness of the chip is decreased to less than 200 μm. When the thickness of the chip is decreased to 50 μm, the maximum value of the residual stress is about -120 MPa. This is because of the decrease of the cross-section of the chip mounted on an organic substrate with high coefficient of thermal expansion. The amplitude of the residual stress is almost constant of about 0 MPa.

On the other hand, in the chip mounted using flip-chip technology, the amplitude of the residual stress is almost constant of about 90 MPa regardless of the thickness of the chip. However, when the thickness of the chip is decreased to less than 200 μm, the maximum value of residual stress is decreased and it reaches about -250 MPa when the thickness is 50 μm. Such a change of the residual stress cause the shift of electronic functions of semiconductor devices easily. Therefore, the thickness of the chip is the important structural factor to assure the constant performance of products. In addition, the height of a bump, the width of a bump, the period of bumps and the thermal expansion coefficient of underfill material are found to be the other important structural factors that determine the distribution of the

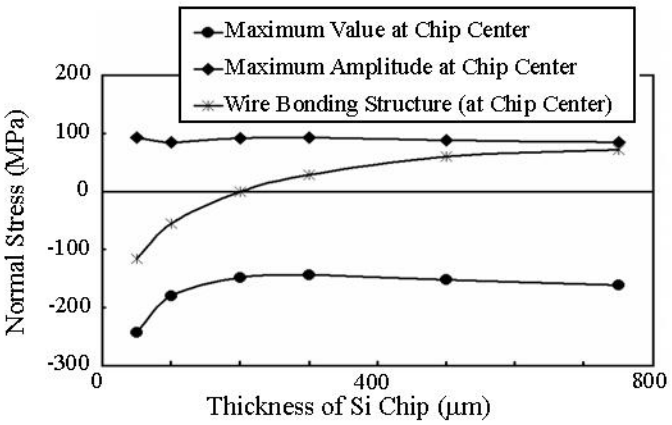

Figure 4. Effect of thickness of a Si chip on residual stress on a transistor formation surface of a Si chip mounted on a substrate by an area-arrayed bump structure and wire bonding structure.

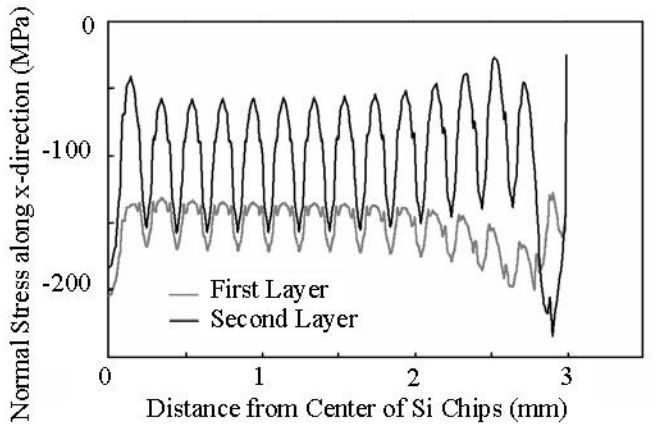

Figure 5. Distribution of the normal stress along x-direction in each Si chip of the same bump alignment model.

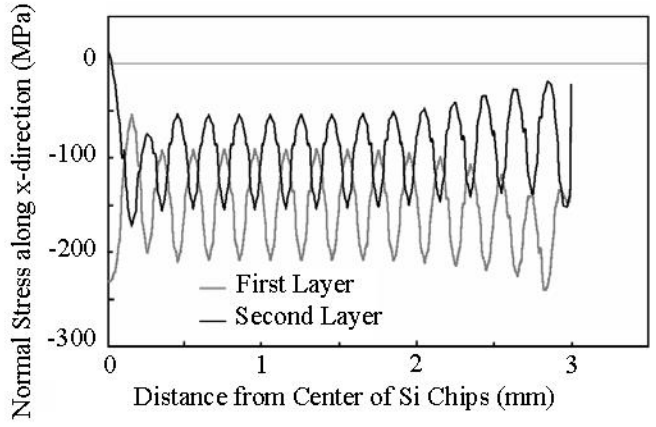

Figure 6. Distribution of the normal stress along x-direction in each Si chip of the different bump alignment model.

residual stress by finite element analyses.

2.4 Residual Stress Distribution in Stacked Two Chips Mounted using a Flip Chip Technology with Area-arrayed Metallic Bumps

The distribution of the normal stress along x-direction on a transistor formation surface of each chip of two-chip-stacked model is shown in figures 5 and 6. Figure 5 is used the same bump alignment model shown figure 2(a). Figure 6 is result of the different bump alignment model shown figure 2(b). In these analyses, the width of each chip is assumed to be 100 μm and the width and the height of Cu bumps are fixed at 100 μm and the pitch of the bump is assumed to be 200 μm. From the analysis result of the same bump alignment model shown figure 5, the clear periodic stress distribution appears in each chip due to the periodic alignment of metallic bumps. However, the maximum value of the residual stress in both chip are different. The stress in the upper chip is about -150 MPa, and the residual stress in the bottom chip is about -170 MPa. Furthermore, the amplitude of the residual stress in an upper chip is about 100 MPa, while the amplitude of the residual stress in the bottom chip is about 40 MPa. The average residual stress in the stacked two chips changes due to the distance from a bending neutral axis of the stacked structure. In addition, the amplitude of the residual stress of the bottom chip located in between the upper chip and the substrate is decreased drastically because the local deformation of the bottom chip is restricted strictly by bumps in the upper layer and the bottom layer.

On the other hand, it was found that the distribution of the residual stress in the bottom chip changes drastically depending on the relationship of the alignment of bumps between the upper layer and the bottom layer. Figure 6 summarizes the distribution of the residual stress in both chips stacked using the different bump alignment structure. The stress distribution of the upper chip does not change. However, the amplitude of the periodic stress of the bottom chip increases drastically and the value is almost the same as the upper chip. The reason for the difference in the average residual stress in the stacked two chips is the difference in the distance from a bending neutral axis of the stacked structure as was explained above. The maximum value of the residual stress in the bottom chip is about -210 MPa, the amplitude of the residual stress in the bottom chip is about 120 MPa. Both value increase significantly comparing with the result obtained from the analyses using the same bump alignment model. Therefore, it can be concluded that the residual stress in the upper chip does not depend on the bump alignment. However, residual stress in the bottom chip changes drastically depending on the difference in the bump alignment between the upper and bottom interconnection layers. The main reason for this bump alignment dependence of the residual stress is the local deformation of the bottom chip. Though the local deformation of the chip stacked using the same bump alignment structure is strictly limited by the bumps in the upper and the bottom layers, the local deformation of the chip stacked in the different bump alignment structure is not restricted by bumps. According to this analysis result, it is concluded that it is very important to optimize not only the thickness of a chip, but also the position (layout) of bumps, to optimize the residual stress in stacked plural chips.

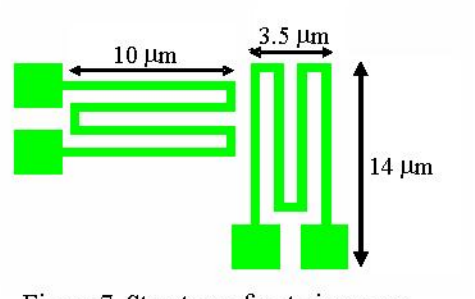

Figure 7. Structure of a strain gauge.

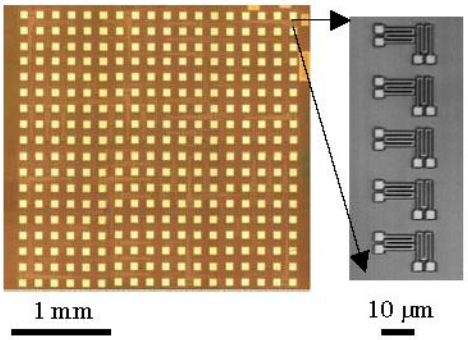

Figure 8. Outlook of a stress sensor chip.

3. Residual Stress Measurement Using a Stress Sensor Chip

In order to prove the existence of the predicted periodic distribution of the residual stress in a Si chip, stress sensor chips were developed using a polycrystalline silicon thin films by applying the piezoresistive effect of silicon [8]-[11]. The average grain size of the polycrystalline film was less than 0.1 μm. A basic structure of strain gauges is shown in Fig. 7. The length of each gauge is 10 μm to measure the distribution of residual stress between two bumps that are apart from 100 μm with each other. The width of the gauge is 0.5 μm. The total length of each gauge is about 40 μm. The sheet resistance of the film was controlled by ion implantation of P, and it was about 420 Ω/square. Thus, the average resistance of each gauge was about 40 kΩ. These gauges were made of an 1-μm

thick polycrystalline film that was deposited on a thermally oxidized silicon wafer.

296 gauges were formed on a 4 mm x 4 mm Si chip as shown in figure 8. 324 Cu bumps are area-arrayed on a chip by electroplating. Both the width and the thickness of the bump are 100 μm, and the interval of the bump is also 100 μm. 5 gauges are formed between the two bumps at most. 168 gauges can be used at a one chip. The gauges of interest are connected to the bumps by thin film interconnection. This stress sensor chip was mounted on a substrate made of a Si wafer.

The mounted sample was bended to simulate the thermal deformation of the stacked structure by applying a four-point bending method as shown in figure 9. The applied strain was monitored by three strain gauges adhered to the back surface of the bending beam. The beam was bended by screws fixed at the both edges of the beam. The symmetry of the loading condition was controlled by balancing the output of the adhered gauges. The change of the resistance of each gauge was measured by contacting proves as shown in the figure. The resistance change of each gauge was measured under an uni-axial tensile stress loading condition. During the stress measurement, the ambient temperature was controlled at $30\pm0.1^{\circ}C$.

Figure 10 shows an example of the measured stress distribution of a sensor chip between two bumps. In this example, the average applied strain at a surface of the sensor chip is about 0.08%, and it causes the average surface stress of about 50 MPa. The vertical axis of this figure is normal stress parallel to the applied stress and the horizontal axis shows the distance from an edge of one bump. The local stress distribution appears between two bumps clearly. The maximum stress of about 90 MPa occurs at the center area between the bumps. The normal stress decreases monotonically to the average stress toward the edge of each bump. Similar stress distribution was observed everywhere at the surface of the sensor chip. This local stress distribution was caused by local deformation of the sensor chip adhered to a substrate using area-arrayed bump structure.

In order to verify this measurement result, the local stress distribution at the surface of a sensor chip was analyzed by applying a three-dimensional finite element analysis. Figure 11 shows the comparison of the measured stress with the calculated result. In this figure, only the difference of the local stress from the average stress is summarized. The horizontal axis of this figure is the distance from the edge of one bump, and the left side bump is close to the center of a sensor chip. The calculated stress distribution is not symmetric between the bumps because of the macroscopic bending of the chip. The measured results are also plotted in

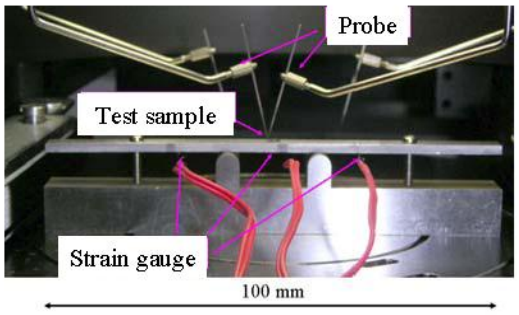

Figure 9. Uni-axial tensile stress loading by a four-point bending method.

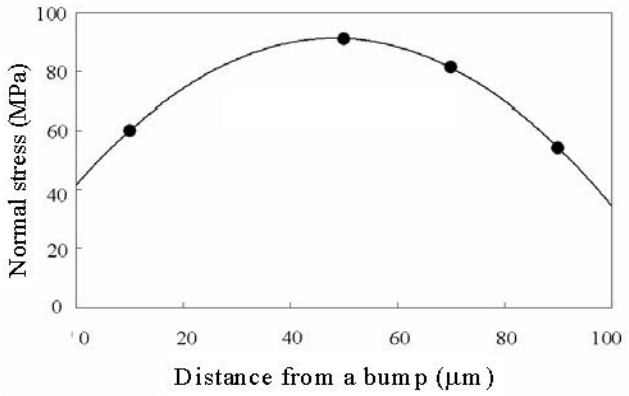

Figure 10. Stress distribution of a Si chip between two Cu bumps caused by bending of a mounted sample. The average strain at a surface of the chips is about 0.08%.

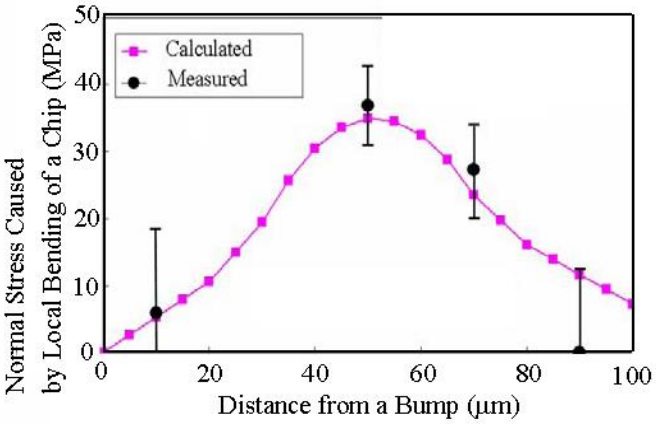

Figure 11. Comparison of the measured stress with a calculated result.

this figure with error bars. Each error bar indicates the maximum and the minimum values among 20 samples. The maximum fluctuation of the measured results is about 10 MPa. The measured results agree well with the calculated results. The maximum difference between the average measured results and the calculated one is about 10 MPa. Therefore, we

have proved the existence of a periodic distribution of the residual stress in a Si chip and validate the analysis results using the finite element analysis.

4. Conclusions

A finite element analysis was performed to make clear the residual stress in stacked chips mounted by flip chip technology using area-arrayed metallic bumps quantitatively. The maximum value of the normal stress on a transistor formation surface of a chip changes about 200 MPa by changing the assembly structure from WB to FC. A periodic stress distribution with amplitude of about 90 MPa also appears due to the periodic alignment of the metallic bumps. Such a change of the residual stress in an LSI chip causes a shift of electronic functions of semiconductor devices in a local area in the chip. The important structural factors that determine the distribution of the residual stress are found to be the thickness of a chip, the height of a bump, the width of a bump, the period of the bumps, and the thermal expansion coefficient of underfill material. The average residual stress in the stacked two chips changes depending on the distance from a bending neutral axis of the stacked structure, and the local residual stress also varies depending on the relative position of bumps between the upper interconnection layer and the bottom interconnection layer. Therefore, it is very important to optimize the thickness of a chip, the position (layout) of bumps, and other structural factors to minimize not only the average residual stress but also the amplitude of the periodic stress. Finally, the estimated stress distribution was proved quantitatively by the experiment using stress-sensing chips with 10-μm long gauges.

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