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A Josephson field effect transistor using an InAs-inserted-channel In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As inverted modulation-doped structure

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A Josephson field effect transistor (JOFET) was coupled with a two-dimensional electron gas in a strained InAs quantum well inserted into an In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As inverted modulation-doped structure. The characteristics of this JOFET are much improved over previous devices by using a high electron mobility transistor (HEMT)-type gate instead of the usual metal-insulator-semiconductor (MIS)-type gate. The superconducting critical current as well as the junction normal resistance are completely controlled via a gate voltage of about $-1$ V; this provides voltage gain over 1 for a JOFET. © 1996 American Institute of Physics.

There have been many attempts to develop a Josephson field effect transistor (JOFET) since the idea was first proposed. 1,2 In this device, the superconducting proximity effect in the normal channel between two superconducting electrodes is controlled by gate voltage. This results in changes in both the superconducting critical current and normal resistance. The operating principle is similar to that of normal FETs. In the early stages of development, a JOFET was achieved using several semiconductor materials such as $p$-type InAs, 3 $p$-type Si, 4 AlGaAs/n-GaAs heterostructures, 5 and InGaAs $p$–$n$ junctions. 6 However, controllability of these devices by gate voltage was rather low.

Recently, we have obtained a supercurrent in a Josephson junction that was coupled with a high-mobility two-dimensional electron gas (2DEG) in a strained InAs quantum well inserted into an In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As modulation-doped structure. 7,8 This InAs-inserted-channel InAlAs/InGaAs heterostructure is an attractive candidate for a JOFET because the 2DEG in the channel has both high sheet-carrier density and high electron mobility. These provide a long mean free path $l$ and normal coherence length $\xi_N$ of the semiconductor. Moreover, a good electrical superconductor–semiconductor contact can be expected because $n$-type InAs has no Schottky barrier at its interface with superconducting metals. Very recently, we reported on research concerning an InAs-inserted-channel InAlAs/InGaAs inverted modulation-doped (i-MD) heterostructure-coupled Josephson junction with a metal-insulator-semiconductor (MIS)-type gate. 9,10 Three-terminal operation was achieved, i.e., the superconducting critical current, $I_C$, as well as the junction normal resistance, $R_N$, were controlled by gate voltage. However, the controllability of this device by gate voltage was no better than that of other JOFETs because of the interface levels at the gate-insulator/semiconductor interface.

In this letter, we report on highly improved characteristics of a JOFET, obtained using the same heterostructure with a high electron mobility transistor (HEMT)-type gate configuration instead of an MIS-type gate configuration. The HEMT-type gate configuration has a gate that is fabricated directly on the top layer of the heterostructure. This type of JOFET was thought to be free from the interface-level problem at the gate-insulator/semiconductor interface. The device structure studied in this letter provides new quantum effects. These concern Fabry–Pérot interference of the critical current 11 and the quantization of the critical current 12 in a superconducting quantum point contact. 13

Figure 1 shows the structure of the JOFET with an InAs-inserted-channel inverted HEMT structure. The heterostruc-

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FIG. 1. The structure of a JOFET with an InAs-inserted-channel inverted HEMT structure: (a) cross-sectional view and (b) electrode configuration.
tute used in this study was grown by molecular beam epitaxy (MBE) on an Fe-doped semi-insulating (100) InP substrate. All InGaAs and InAlAs layers were lattice matched to InP. The growth temperature for all layers was kept at about 300 °C, since the critical thickness increases at lower growth temperatures. Using the results from our previous reports, we fixed the InAs quantum-well thickness at 4 nm and the insertion position (the distance between the InAlAs spacer layer and the InAs quantum well) at 2.5 nm. In this way, a 2DEG was confined in the inserted InAs layer. Length $L$ between Nb electrodes was chosen to be in the range of 0.2–1.0 μm, and the gate length $L_g$ is 0.1 μm.

The fabrication process can be briefly described, while details of the device fabrication are reported elsewhere. First, two 100 nm thick superconducting Nb electrodes were defined by a liftoff process employing electron beam lithography. Chemical etching with an HF-based etchant was used to remove the 20 nm undoped InAlAs layer. The layers from the 13.5 nm undoped InGaAs to the 6 nm undoped InAlAs were etched by rf sputter cleaning in an evaporation chamber. The two Nb electrodes were then angle-deposited by electron beam deposition to make a good contact between Nb electrodes and the sidewall of the InAs layer. Length $L$ between the Nb electrodes was chosen to be in the range of 0.2–1.0 μm on the same chip, and the electrode width $W$ was 40 μm. Next, after mesa etching for device isolation with a citric-acid-based etchant, the SiO$_2$ passivation film was deposited and lifted off using the resist pattern for the mesa etching. Resist pattern for the gate portion was then made by electron beam lithography. When the $L$ was about 0.2 μm, gate length $L_g$ and the position deviation allowance had to be shorter than 0.1 and 0.05 μm, respectively. Finally, the Al gate metal was deposited on the undoped InAlAs layer and lifted off. The $L_g$ was set in the range of 0.08–0.2 μm. We successfully fabricated a gate with $L_g=0.1$ μm in the $L$ of 0.3 μm. This is shown in Fig. 2.

![Al gate](image)

**FIG. 2.** SEM microphotograph of the InAs-inserted-channel superconducting HEMT. The length $L$ between Nb electrodes is 0.3 μm and the gate length $L_g$ is 0.1 μm.

The current–voltage ($I$–$V$) characteristics of the device with $L=0.35$ μm and $L_g=0.1$ μm at 1 K were observed by changing the applied gate voltage $V_g$ from 0 to −1.1 V (Fig. 3). The supercurrent flowed through the 2DEG due to the superconducting proximity effect. Sheet carrier density $n_s$ and mobility $\mu$ for the 2DEG in this device were measured at 10 K as $2.3 \times 10^{12}$ cm$^{-2}$ and 111 000 cm$^2$/V s, respectively, by Hall measurement. Figure 4 shows the measured $I_C$ and $R_N$ at 1 K as a function of gate voltage. Figures 3 and 4 clearly show that $I_C$ was reduced and $R_N$ increased by increasing the absolute value of the applied gate voltage. The $I_C$ for this type of junction structure is very sensitive to magnetic fields. Therefore, for each gate voltage, the maximum $I_C$ was specified by carefully optimizing $I_C$ with the help of a weak magnetic field applied perpendicular to the 2DEG. Over the range from 0 to −1.15 V, the magnitude of the applied magnetic field that maximized $I_C$ was constant. An $I_C$ of about 5 μA and an $R_N$ of 16 Ω were obtained at $V_g=0$ V. The $I_C$ was almost completely suppressed at $V_g=−0.9$ V and $R_N$ was increased to 1.46 MΩ at $V_g=−1.15$ V. Note that no gate-leakage current was observed at $V_g=−1.15$ V. These results show a remarkable improvement in controllability of both $I_C$ and $R_N$ via gate voltage, compared with the JFET that used the MIS-type gate. This is because the interface between the gate electrode and the undoped InAlAs layer is free from the interface levels, while SiO$_2$ was used as the gate insulator in the MIS-type gate with the interface levels at the SiO$_2$/InAlAs interface.

Next, we shall discuss the high device performance in terms of superconducting transconductance and voltage

![Graph](image)

**FIG. 3.** Current–voltage characteristics under applied voltage ranging from 0 to −1.1 V.

**FIG. 4.** Measured critical current and the junction’s normal resistance at 1 K as a function of gate voltage.
gain. The superconducting transconductance \( g_m^s \) is defined as

\[
g_m^s = \frac{dI_C}{dV_g},
\]

where \( I_C \) is the value of \( I_C \) when \( W \) is 1 mm. The maximum \( g_m^s \) for the device was about 350 \( \mu \)S/mm at \( V_g \sim -0.7 \) V. This value is about six times as large as that of the MIS-type gate JOFETs.\(^{9,10}\) The voltage gain \( G \) is given by an inverter circuit: \(^{19}\)

\[
G = \frac{I_C^m R_L R_{N}^{\text{off}} \left(R_L + R_{N}^{\text{off}}\right)}{V^*_{g} - V_{g}^{\text{on}}},
\]

where \( I_C^m \) and \( V_{g}^{\text{on}} \) are the critical current and the gate voltage in the superconducting state (on state), \( R_{N}^{\text{off}} \) and \( V_{g}^{\text{on}} \) are the normal resistance and the gate voltage in the resistive state (off state), and \( R_L \) is the load resistance. When \( R_{N}^{\text{off}} = 1.46 \) M\( \Omega \) at \( V_g = -1.15 \) V and \( I_C^m = 5 \) \( \mu \)A at \( V_g \sim 0 \) V are adopted, the maximum \( G \) value was calculated to be approximately 4 for \( R_{N}^{\text{off}} = R_L \). If the condition \( R_{N}^{\text{off}} > R_L \) is required for the circuit operation, the \( G \) value becomes 1 for \( R_L = 200 \) k\( \Omega \). By comparing these calculated values of \( G \) with \( G \) of \( \sim 10^{-5} \) for an MIS-type gate JOFETs\(^{9,10}\) and \( \sim 3 \times 10^{-3} \) for JOFETs using \( p \)-type Si\(^{4}\) or \( p \)-type InAs,\(^{20}\) we established that the so-called voltage gain was obtained for the first time in a JOFET. This was because a very high \( R_{N}^{\text{off}} \) was obtained due to the high-gate voltage controllability of the HEMT-type gate. It should be noted that an \( I_C \) value of about 100 \( \mu \)A was obtained for the previously reported junction with \( W = 80 \) \( \mu \)m using the same heterostructure.\(^7\) Therefore, when the JOFET studied here has almost the same magnitude of \( I_C \), it is possible to obtain a \( G \) value of 10 for \( R_L = 200 \) k\( \Omega \) and of 1 even for \( R_L = 20 \) k\( \Omega \). On the other hand, a switching time \( \tau_s \) of about 40 ps was evaluated from the product of the gate capacitance \( C_g \) and \( R_L \), when \( C_g \approx 20 \) f\( \text{F} \) was estimated from the gate area and the InAlAs gate Schottky layer thickness, and \( R_L = 20 \) k\( \Omega \). This value of \( \tau_s \) is not fast, compared with a conventional Josephson junction (JJ). In order to reduce \( \tau_s \), both \( C_g \) and \( R_L \) should be decreased by a reduction of \( L_g \) and an increase in \( I_C \). When \( C_g = 10 \) f\( \text{F} \) and \( R_L = 1 \) k\( \Omega \), it is possible to obtain \( \tau_s \) of 10 ps, which is almost the same as a conventional JJ. \( C_g \) of 10 f\( \text{F} \) can be obtained when \( L_g \) is 50 nm. \( R_L \) of 1 k\( \Omega \) can also be obtained when \( I_C \) is 1 mA for \( W = 40 \) \( \mu \)m. The JJ using the InAs/AlSb heterostructure has the \( I_C \) of about 5 mA for \( W = 40 \) \( \mu \)m,\(^{21}\) which has almost the same structure as our JOFET. Therefore, our JOFET with \( I_C \) of over 1 mA will be achieved by optimizing the Nb/InAs contact, and we believe that it is possible to obtain \( \tau_s \) of under 10 ps in the future.

In conclusion, we fabricated a JOFET by using an InAs-inserted-channel InAlAs/InGaAs inverted modulation-doped structure. We also demonstrated the much improved characteristics of the device obtained by using an HEMT-type gate, instead of an MIS-type gate. Both the superconducting critical current as well as the junction normal resistance were completely controlled via the gate voltage of \( \sim -1 \) V. Moreover, the superconducting transconductance and the voltage gain were highly increased in comparison with previous JOFETs.

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