Fluxoid motion in phase mode Josephson switching system

Nakajima K., Oya G., Sawada Y.

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Abstract

We have investigated the possibility of the phase mode operation, i.e. the mode to transfer the fluxoid, not to transfer the voltage pulse, of Josephson switching system by fabricating a resistively coupled D.C. SQUID's array and 4J-loop which are expected to be advantageous in miniaturization by using its large kinetic momentum effect. The threshold characteristics of these superconducting loops and its LI dependence agreed with the theoretical predictions. The phase mode logic actions were verified to operate really in a resistively coupled D.C.SQUID's and a coupled D.C. SQUID with a 4J-loop. A computer simulation showed that a resistively coupled SQUIDs array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown a total system configuration of the phase mode operation. For the power loss and the information processing speed, the phase mode was verified to have an advantage over the ordinary voltage mode by two orders of magnitude.

Introduction

We have investigated in this paper the possibility of the phase mode operation of Josephson switching system by fabricating a resistively coupled D.C.SQUID's array and 4J-loop's which are superconducting loops containing four series Josephson junctions and show large kinetic momentum quantum effect. The voltage mode devices which are actively being investigated and constructed nowadays depend for its operation on the existence of two stable current carrying states at $V=0$ and $V=\Phi_0/2$. On the other hand the phase mode devices depend on many stable states separated from each other by $2\pi$ in the phase difference plane. In the phase mode all logic function can be achieved by using the interactions between fluxoids which are employed as information bits without occupying voltage states. Although two kind of phase mode action have already been reported as flux shuttle and soliton device by using continuous Josephson lines, we report in this paper the first phase mode operation in the circuits constructed by D.C.SQUID and 4J-loop where one can expect higher density system. To study the difference in characteristics of the two modes, a computer simulation was done for a resistively coupled nonsymmetrical D.C.SQUID's array which showed that a resistively coupled SQUID's array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown an example of total system configuration of the phase mode operation.

Fabrication and characteristics of basic elements

We have fabricated D.C.SQUID's and 4J-loop's by using Pb alloy and rf plasma oxidation. The fabrication process is the following, 1), a 4000A-thick niobium layer is deposited on a Si wafer by electron beam evaporating, 2), the surface of niobium layer is anodized by 1000A, 3), SiO is deposited as an insulating layer with a thickness of 3000A, 4), 1000A thick resistors are deposited using AuIn alloy, 5), a 1500A-thick base-electrode is formed by sequential evaporation of gold, lead, and indium, 6), a SiO layer with thickness of 3000A is formed to demarcate the circular junction areas, 7), A tunneling oxide barrier is formed by rf plasma oxidation method. A 4500A-thick counter electrode is deposited by the successive evaporation of lead, gold, and lead. The 4J-loop we have fabricated has four junctions of 5 µm diameter. The minimum line width of the pattern is 10 µm.

The most basic characteristics of 4J-loop's are threshold patterns which demarcate the voltage states and the non-voltage states of 4J-loop's. Figure 1 shows the calculated threshold patterns of a 4J-loop by using a linearized approximation. The equivalent circuit is shown in the inset. In the figure the I's of the four junctions are same, the parameter is the value of LIc, and the diamond-shaped patterns or triangle patterns show the quantum states of the loop. If LIc<Φ0, the quantum states more than quantum number n=2 do not exist in contrast with D.C.SQUID.

**Fig.1.** Threshold curves of a 4J-loop calculated by using the inset equivalent circuit and linearized approximation.

In order to obtain a threshold curve experimentally, we must observe all the junctions voltages. At present time we measure each junctions voltage individually, after that we superpose every pattern to get the whole threshold curve. Figure 2 shows the observed threshold curve where voltages of two junctions were measured. The two junctions correspond to $J_1$ and $J_2$ junctions shown in the equivalent circuit in Fig. 1. The whole threshold curve is shown in Fig. 3. LIc was estimated to be ~0.36Φ0 from the measurement of D.C.SQUID which was fabricated in the same pattern as the 4J-loop. This estimation agrees with the theoretical prediction of Fig. 1. It can be seen from Fig. 3 that only three quantum states n=0,1,2 exist in contrast with D.C.SQUID where there are many quantum states even though LIc is smaller than Φ0. These quantum states and vortex transitions in the loop are used when the logic circuits...
Experimental logic operation

We have fabricated elementary logic circuits of phase mode system which are constructed of the resistively coupled D.C. SQUID's or 4J-loop's. Figure 4 shows a 2-input phase mode logic circuit consisting of four D.C. SQUID's connected by AuIn alloy resistors, and its equivalent circuit. The each circular Josephson junction has a diameter of 8 \( \mu \)m and minimum line width is 10 \( \mu \)m. This circuit was constructed to confirm SHIFT, OR, and AND logic operations in phase mode.

As the first step of logic operation, resistively connected D.C. SQUID's 2 and 3 of the circuit were used to examine the shift of a single fluxoid from 2 to 3. Figures 5(a) and 5(b) show the threshold curve of SQUID 2 and I-V characteristics of SQUID 3, respectively. Figure 6 shows the threshold curve of SQUID 2 and 3 shown in Fig. 4, respectively. Notice that the voltage mode operation was also verified to be achieved in our circuits as GIL gates by changing bias current and control current conditions. For a comparison the voltage mode operation in the same circuit is shown in Fig. 6(b). Notice that Vd appears in the existence of both Vg and Vd. The SHIFT logic operation shown in Fig. 6(a) is also achieved by using SQUID 1 and 3, so this operation corresponds to OR logic in the phase mode.
Fig. 6. (a) Experimental SHIFT or OR logic operation in the phase mode circuit shown in Fig. 4. (b) Voltage mode operation in the same circuit.

An AND logic operation in the phase mode is shown in Fig. 7. Notice that Vd appears in the existence of both Ig1 and Ig2 which are the control currents of SQUID 1 and 2, respectively. It was confirmed in this measurement that Vd did not appear, when either Ig or Ig2 was reduced to zero. In this case the value of the connecting resistor was so small (~0.08 Ω) that the generators voltage appeared by the reflection from the detector.

These phase mode action have also been observed in a circuit of a resistively coupled D.C.SQUID and a 4J-loop. In order to confirm the phase mode operation, a Josephson sampling system are being prepared.

Phase mode operation separated from voltage mode

To study the difference in characteristics of the two modes, a computer simulation was done for a resistively coupled nonsymmetrical D.C.SQUID's array which are ordinarily used as the voltage mode devices as shown in Fig. 8. This circuit acts on both the phase mode and the voltage mode depending upon the circuit parameters. The phase and the voltage mode actions in the same circuit are separated from each other in the circuit parameter plane, having a clear boundary as shown in the same figure where γ=Ib/Ic, α=2Rc(2mLcC/αIc)1/2, Γ=Q(2Rc/2mLcC)1/2, 2mLc=0.5αγ, 2mL1c=0.4γ. γ and α denote the phase and the voltage mode regions respectively. □ denotes the signal attenuation region. It can be seen from the figure that the phase mode operation can be achieved in the region of smaller γ compared to the voltage mode operation. The voltage hold time in the phase mode is nearly equal to the switching time of a junction ~100ps, but in the voltage mode that is equal to the cycle time ~ns owing to the latching mode. Therefore, for the power loss and the information processing speed and density, the phase mode system have an advantage over the voltage mode system more than two order.

Fig. 7. Experimental AND logic operation in the phase mode circuit shown in Fig. 4.

Fig. 8. Signal transport regions in the circuit parameter plane which circuit is shown on the upside. ○ and △ denote the phase and the voltage mode regions, respectively. □ denotes the signal attenuation region.

Total phase mode computer system

Individual logic functions of the phase mode system have been already proposed by us.6 But systematic computer operations in the system has not been investigated yet. The system operation in the phase mode is largely different from in the ordinary voltage mode which is similar the one used in a computer system constructed by semiconductor devices. We present a simple but total phase mode Josephson computer system in this section. The computer is binary and asynchronous. Word length is 6 bits. The instruction format consists of the 3-bit operation-code part and the 3-bit address part. So capacity of memory is 48 bits. Available instructions of the machine is 7. The number of Josephson junctions to be used in the computer is estimated to be about 8000, without counting the parts of signal transmission lines. In the system five elements to be constructed by oxide tunnel junctions are used which are D.C.SQUID, 4J-loop, resistor, discrete Josephson transmission line (DJTL), and trigger turning

Fig. 9. System configuration of a phase mode Josephson computer.
**Instruction**

**Address**

Fig. 10. Control unit of the phase mode Josephson computer system shown in Fig. 9.

Instruction

**Point (Tpt)**. Figure 9 shows the configuration of the computer where I, C, CU, M, IV, A, O, T-I, and T-II denote input, counter, control unit, memory, inverter, adder, output, terminal I and E, respectively. S and W are signals to start the machine and to store data in the memory by manual, respectively. Lines with arrows, circles, and broken line denote DJTL's, Tpt's, and resistor. Solid circles mean setting operations of a single fluxoid. For example, the control unit is shown in Fig. 10 where double squares denote the function shown in Fig. 11. The bold line used in Fig. 11(1) denotes a annihilation function of two colliding fluxoids as shown in its right hand side. Squares denote 4J-loop's. The function of Fig. 11(1) is explained by using the truth table also shown in this figure, namely, the propagating direction of fluxoid from I is switched to the output a or b depending upon the fluxoid setting at the 4J-loop. It is expected that this function is also accomplished by the construction of Fig. 11(2). The symbol which is used to denote this function is the right hand side in the figure. The control unit shown in Fig. 10 as same as the other computer elements in our system is constructed by using many basic elements shown in Fig. 11. The address part of the control unit is connected with the memory. The basic method of the machine operation is that the propagating directions of a single fluxoid are controlled by the single fluxoid setting at a 4J-loop on the way of the propagating fluxoid. A more detailed explanation of the machine operation will be presented in a forthcoming paper.

**Conclusion**

We have investigated the possibility of the phase mode operation of Josephson switching system by fabricating a resistively coupled D.C.SQUID's array and 4J-loop which are expected to be advantageous in dense packing by using its large kinetic momentum effect. The threshold characteristics of these superconducting loops and its Ic dependence agreed with the theoretical predictions. The phase mode logic actions SHIFT, OR, and AND were verified to operate really in a resistively coupled D.C.SQUID's and a coupled D.C.SQUID with a 4J-loop. A computer simulation showed that a resistively coupled SQUID's array acts both on phase mode and voltage mode by changing the circuit parameters, but that the two modes are clearly separated in a parameter space. Finally we have shown a total system configuration of the phase mode operation. It is roughly estimated that the machine will provide about 200MFLOPS computing power. The power loss is about 10^-7w/gate, and is about pW in the total system without counting the dissipation of current source part. It would be expected that for utilizing fluxoids as information bits the phase mode system is more favourable to data flow machine than voltage mode system.

**References**

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Fig. 11. Basic elements of the phase mode computer system. Squares denote 4J-loop's. S and I denote a setting fluxoid and a input fluxoid, respectively. a and b are two outputs. Circuits (1) and (2) have the same function which is explained by the truth table inset in this figure. The right side figure is a symbol for the circuits.