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論文内容要約

Abstract

The recent miniaturization of computers and networking gear has again attracted world-wide attention in research on ubiquitous computing that has been aimed at ideal systems to support human activities. Ubiquitous computing, which has also been known as machine to machine (M2M) or the Internet of things (IOT) in recent years, is one of the ideal goals of engineering to achieve health, welfare, and public safety by using knowledge in advanced science. Sensor networks are considered to be core technologies of IOT and M2M that are expected to achieve ideal equipment or environments that all everyone can use regardless of their age, abilities, situation, or status in life.

Remote healthcare and telemedicine are two of the expected applications of sensor networks. Telemedicine has contributed to health management such as continuous monitoring of health conditions, diagnosis by medical specialists, and prevention of illnesses from worsening. It has become possible for patients everywhere who are wearing wireless sensor nodes to be diagnosed at any time and from anywhere from remote places.

Wireless sensor nodes have recently been produced by combining microprocessors, wireless communication modules, batteries, energy harvesting devices, and power supply modules. Although such modules in which necessary functions can be freely rearranged are the best for prototyping and proving tests, it has been difficult to ensure reliability and achieve lower power consumption because combinations of numerous devices have led to high failure rates and modules have not yet been designed to cooperate with one another.

In contrast to digital equipment that uses system on a chip (SoC), wireless mobile equipment such as mobile phones and wireless sensor nodes have many semiconductor chips installed because it is difficult to create high-quality digital, power supplies, and radio frequency (RF) circuits on silicon chips. High levels of reliability and long battery life are crucial for healthcare and telemedicine devices compared with consumer electronics. Wireless sensor nodes using SoC including all function blocks raise the possibility of achieving high levels of reliability, low power consumption, miniaturization, and high

levels of performance due to their total design and optimization. This dissertation reports on research results obtained from process technology that make it possible to integrate high-performance logic, high-density memories, RF circuits, and power supply circuits on one chip and reports the effects of total design on further energy savings.

Ultralow-power embedded memory technology was proposed in Chapter 2. This chapter discusses the impact of the integration of DRAM processes on the performance of transistors and the complexity of processes when SoCs were fabricated by using conventional MIM capacitor DRAM technology. The fabrication process for DRAMs did not affect the performance of transistors by using low-temperature processes including new deposition materials and MIM capacitors. MIM capacitors with new forms of SiN deposition, however, need special materials to fabricate them and additional process steps. A new type of embedded memory that does not require special materials or additional process steps is proposed to solve these problems. It was clarified that the proposed memory cell did not require any capacitor structures and had good process compatibility with logic process and ultra-low-power write operation.

Capacitor-less 1T-DRAMs seem most promising in terms of their capacity, speed, and structural complexity of embedded memory. Drain current could be lowered more remarkably than when using impact ionization current by using gate-induced drain leakage (GIDL) current to write the “1” state. The use of GIDL current in write “1” operation achieved power consumption that was four orders of magnitude lower than that in the use of impact ionization current, which led to operative power reductions. The capacitor-less 1T-DRAM could read and write within several nanoseconds by using GIDL current, and had a larger sense margin than that by using impact ionization current due to an increase in the number of accumulated holes, which was caused by the negative body potential in write operation. The disturb margin, which is important for selective read and write operation, is discussed in detail for the memory function in this paper, and it was clarified that the 1T-DRAM using GIDL current had enough disturb margin for all operations.

The issue of scaling 1T-DRAM cells below 50 nm is then discussed. It was confirmed through device simulations that scaling down L_g to less than 100 nm was quite difficult for conventional 1T-DRAMs due to pn-junction leakage current. Higher concentrations of channel impurities are required to suppress short-channel effects to make the 1T-DRAM scalable and this should significantly degrade retention characteristics. A double-gate fully depleted FinFET DRAM (DG-FinDRAM) is proposed to overcome this problem. The DG-FinDRAM had a body with very low impurity concentrations even at a gate length of 50 nm, which led to a long retention time. Moreover, a large sense margin was obtained because of a straight energy-band distribution. It was clarified that DG-FinDRAMs were very promising embedded memories due to their very low impurity concentrations even below the gate length of 50 nm. Capacitor-less 1T-DRAMs offer the possibility of playing the leading role in memories in terms of the capacity, speed, power, and structural complexity of embedded memories.

Chapter 3 describes transistor design and fabrication processes for low-power and highly reliable sensor nodes. New

transistor design and fabrication processes are discussed to simultaneously achieve low-power and high-speed transistors and high-frequency and high-voltage transistors. We need to fabricate low-power and high-performance logic transistors for digital processing and high-frequency and high voltage endurance transistors for RF and power supply circuits. Digital processors process information collected by sensors and then RF circuits transmit the processed data to base stations. Power supply circuits provide stable power sources to processors, RF circuits, and sensors. Therefore, the transistors for these circuits should be integrated in a chip to achieve low-power and highly reliable sensor nodes.

Reduced leakage current and increased drive current effectively reduce digital processing power and increase computation speed. Although booster technologies such as stress effects to increase drive current have recently been proposed, the effect of stress is limited in transistors that are aimed at low power consumption in low-power sensor nodes. A new performance index, i.e., characteristic current (I_{chr}), is proposed because the conventional saturation drive current used to estimate the approximate CMOS inverter delay time is inaccurate for deeply scaled devices. Then, a new method of device design based on I_{chr} is discussed to achieve a higher operation frequency for CMOS inverter circuits using low power transistors. The new device design shortens the propagation delay time (T_{pd}) by 15% in 65-nm technology.

High voltage transistor design is also discussed to achieve high-performance power supply and RF circuits. The optimization point for the transistors of RF and power supply circuits in sensor nodes differs from that in digital transistor design to maximize the performance of individual circuits. It is a challenge to fabricate digital transistors and RF or high voltage transistors in a chip even though the best circuit performance is achieved using specialized transistors for individual circuits. It is necessary to simultaneously suppress both hot-carrier degradation and short channel effects to achieve high-performance high voltage transistors. Hot-carrier degradation becomes particularly serious in n-type metal-oxide-semiconductor field effect transistors (nMOSFETs) because impact ionization current clearly increases due to higher lateral electric field. It was clarified that short-channel effects and impact ionization current could simultaneously be controlled by independently adjusting the channel dose and source-side halo dose. By applying an asymmetric structure to 2.5 V transistors, the proposed device that had a laterally modulated channel demonstrated sufficient reliability even during operation at 3.3 V. Since this technology also improved current drivability, the layout area of the high-voltage circuit block could be reduced down to 55% because of the reduced total gate width. Then, a metal-on-gate (MOG) structure is proposed to improve high-frequency characteristics, which did not need any additional processes because the gate contact and first metal wire in the conventional process were used. A higher f_{max} of 55 GHz was successfully obtained by combining MOG and laterally modulated channel structures. Because neither laterally modulated channels nor MOG structures need complex fabrication processes, low-power and high-performance transistors and high-frequency and high voltage transistors can be fabricated on a chip by using 65-nm-node technology.

Low-power transistors, high-frequency transistors, and high-voltage transistors were simultaneously fabricated on the same wafer and all CMOS RF-SoC instead of III-V based components were successfully achieved as will be explained in Chapter 4. A fully integrated power amplifier in the CMOS process (CMOS-PA) is one of the largest challenges to achieve an ideal RF-SoC, which includes both RF and extensive digital processing. Although fewer parts that are compact are needed to achieve highly reliable sensor nodes, PA is needed to achieve long distance wireless communications in remote health care and telemedicine. The main challenge to achieve CMOS-PA is to improve efficiency, which is currently lower than that in conventional PAs based on III-V compound semiconductors. Fully integrated CMOS PAs are expected for small equipment such as that in wireless sensor nodes because PAs based on III-V need more parts and result in larger footprints. We need to use a kind of 3G or 4G communication technology for future sensor nodes to connect to networks such as the Internet without relatively large hub devices.

Signals in recent wireless standards such as wideband code division multiple access (W-CDMA) and long term evolution (LTE) exhibit high peak-to-average ratios (PAPRs) and wide channel bandwidths. This requires high linearity for PAs to meet the signal quality specifications at the transmitting antenna. Conventional linear PAs can satisfy linearity requirements by operating in large back-off regions. This leads to lower efficiency because PAs operate at lower levels than their saturated output power. Envelope tracking PA (ET-PA) that can operate in the saturated power region by changing the drain voltage according to the envelope of modulated RF signals was proposed by combining CMOS-PA and high-speed CMOS power supply in a chip.

High-efficiency CMOS-PA based on envelope tracking (ET) technology that complied with W-CDMA and LTE was discussed focusing on efficiency and distortion. Asymmetric high-voltage and high-frequency transistors were implemented in linear PA to achieve high levels of transmitting power and efficiency. Combinations of linear PA and high-speed power supply circuits can achieve high-performance ET operations. By adopting a high-speed CMOS envelope amplifier with current direction sensing, a 5% improvement in total power-added efficiency (PAE) and an 11 dB decrease in the adjacent channel leakage ratio (ACLR) were achieved with a W-CDMA signal. Moreover, the proposed PA block achieved a PAE of 25.4% for a 10 MHz LTE signal at an output power (P_{out}) of 25.6 dBm and a gain of 24 dB. It was clarified that the combination of the power amplifier, power supply, and control circuit that were fabricated on the same CMOS chip had the possibility of decreasing the power consumption of sensor nodes.

Finally, Chapter 5 concludes with the results obtained from this work and discusses directions for future research.