Highly Reliable Copper Dual-Damascene Interconnects With Self-Formed $MnSi_xO_y$ Barrier Layer

Takamasa Usui, *Member, IEEE*, Hayato Nasu, *Member, IEEE*, Shingo Takahashi, Noriyoshi Shimizu, T. Nishikawa, Masaki Yoshimaru, *Member, IEEE*, Hideki Shibata, Makoto Wada, and Junichi Koike

***Abstract*—Copper (Cu) dual-damascene interconnects with a self-formed $MnSi_xO_y$ barrier layer were successfully fabricated. Transmission electron microscopy shows that approximately 2-nm thick and continuous $MnSi_xO_y$ layer was formed at the interface of Cu and dielectric SiO_2, and that no barrier was formed at the via bottom because no oxygen was at the via bottom during annealing. No leakage-current increase was observed, and electron energy loss analysis shows that no Cu was in SiO_2, suggesting that $MnSi_xO_y$ layer has sufficient barrier properties for Cu, and that the concept of self-forming barrier process works in Cu dual-damascene interconnects. Via chain yield of more than 90% and 50% reduction in via resistance were obtained as compared with physical vapor deposited tantalum barrier, because there is no barrier at the via bottom. In addition, no failure in the stress-induced voiding measurement was found even after a 1600-h testing. No failure in electromigration (EM) testing was found, as the electron flow is from the lower level interconnects through via up to upper level interconnects even after 1000-h testing. At least, four times EM lifetime improvement was obtained in the case of electron flow from upper level interconnect through via down to lower level interconnects. Significant EM lifetime improvement is due to no flux divergence site at the via bottom, resulting from there being no bottom barrier at the via.**

***Index Terms*—Barrier, Cu-alloy, interconnect, reliability.**

I. Introduction

AFTER introduction of the copper (Cu) damascene or dual-damascene interconnects, physical vapor deposition (PVD) tantalum (Ta) has been widely employed as a barrier metal for Cu [1], [2]. Thickness and coverage of barrier layer affects line resistance and Cu-filling capability into the via and trench. Another aspect of barrier properties is adhesion to dielectric and Cu, which is closely related to the reliability, such as stress-induced voiding (SiV) and electromigration (EM). As the trench width and via diameter shrink below 100 nm, it seems to be difficult to obtain the uniform coverage. On the other hand, although chemical vapor deposition (CVD) of TiSiN was proposed in order to improve coverage [3], [4], CVD TiSiN requires high temperature during deposition, resulting in SiV failure in the lower level interconnects. Moreover, CVD TiSiN has poor adhesion property to the Cu, which causes SiV failure in the via as well. PVD/CVD/PVD layered structure is necessary to suppress the SiV failure [5].

As the trench width and via diameter shrink below 100 nm, atomic layer deposition (ALD) of WC_xN_y layer has been proposed in order to obtain thin and conformal coverage [6]. Unfortunately, since ALD film has poor adhesion property to Cu, PVD/ALD/PVD layered structure is essential from the viewpoint of reliability [7]. Self-forming barrier technology could be one of the promising technologies to satisfy the essential properties of barrier layer. Self-formation technology using a CuX [X = aluminum (Al), germanium (Ge), magnesium (Mg), manganese (Mn), and nickel (Ni)] seed layer was examined by blanket films from the viewpoint of material science [8], [9]. CuMn alloy seed layer was proposed by Koike and Wada [10]. It is also reported that Cu resistivity decreases as the annealing temperature increases, and that Cu resistivity becomes almost the same as that of pure Cu in the case of annealing at over 300 °C using blanket Mn and Cu films [11]. This self-forming barrier technology was applied to the Cu dual-damascene interconnects [12]. In addition, it was recently reported that low-k SiOC/Poly-Arylene(PAr) hybrid dielectric Cu dual-damascene interconnects with self-formed barrier were fabricated successfully [13]. This fact suggests that the self-forming barrier technology using CuMn alloy has application extendibility to the low-k dielectric Cu dual-damascene interconnects.

In this experiment, this self-forming barrier technology was applied to Cu dual-damascene interconnects. Very thin and continuous self-formed barrier $MnSi_xO_y$ layer was realized at the interface between Cu and silicon dioxide (SiO_2) of the interconnect trench and via. Via structure without bottom barrier was also realized in the Cu dual-damascene interconnects, which is able to provide an excellent SiV and EM performance.

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T. Usui and H. Nasu are with the Semiconductor Technology Academic Research Center, Yokohama 222-0033, Japan, and also with the Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki 212-8582, Japan.

S. Takahashi is with the Semiconductor Technology Academic Research Center, Yokohama 222-0033, Japan, and also with Sony Corporation, Tokyo 141-0001, Japan.

N. Shimizu is with the Semiconductor Technology Academic Research Center, Yokohama 222-0033, Japan, and also with Fujitsu Laboratories, Kawasaki 211-8588, Japan.

T. Nishikawa and M. Yoshimaru are with the Semiconductor Technology Academic Research Center, Yokohama 222-0033, Japan.

H. Shibata is with the Semiconductor Technology Academic Research Center, Yokohama 222-0033, Japan, and also with the Advanced BEOL Technology Department, Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki 212-8582, Japan.

M. Wada is with the Department of Material Science, Tohoku University, Sendai 980-8579, Japan, and also with the Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki 212-8582, Japan.

J. Koike is with the Department of Material Science, Tohoku University, Sendai 980-8579, Japan.

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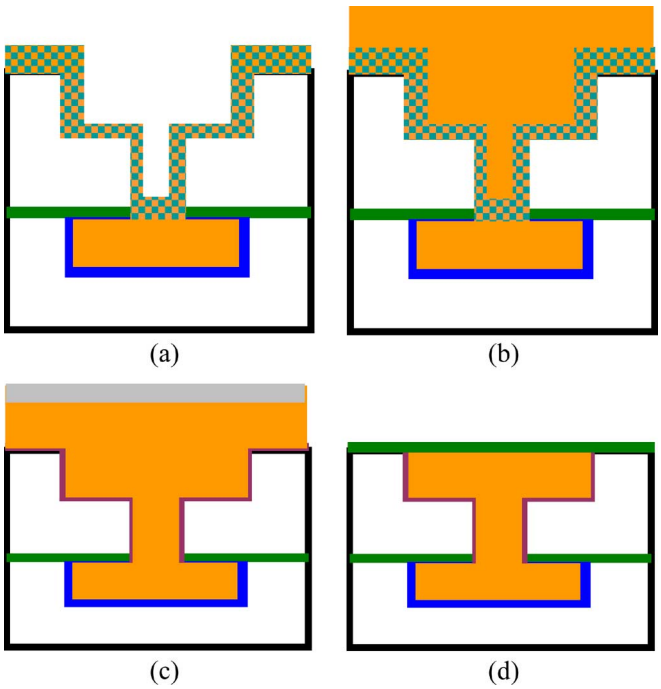

Fig. 1. Schematics of the fabrication process for Cu dual-damascene interconnects with self-formed $MnSi_xO_y$ barrier layer. (a) Deposition of CuMn seed layer by sputtering. (b) Cu deposition by electrochemical plating. (c) Annealing for $MnSi_xO_y$ layer. (d) Removal of excess Cu and Mn by CMP and deposition of dielectric diffusion barrier.

II. Experimental

A. Self-Forming Barrier Process of Cu Dual Damascene Interconnects

Process flow employed in this experiment is as follows, and schematic of self-forming barrier process is shown in Fig. 1.

Process flow of self-forming barrier process:

1) 80-nm thick Cu-2at%Mn alloy deposition by sputtering as a seed layer [in Fig. 1(a)];
2) electrochemical plating [Fig. 1(b)];
3) annealing at 300 °C for 30 min [Fig. 1(c)];
4) Cu and barrier chemical-mechanical polishing (CMP) to remove MnO_x and excess Cu and deposition of dielectric diffusion barrier SiC_xN_y [Fig. 1(d)].

During the annealing, Mn reacts with SiO_2, resulting in the forming of $MnSi_xO_y$ layer at the interface, and excess Mn in Cu will migrate toward the top surface of the Cu and react with oxygen, resulting in the forming of MnO_x. The fact that excess Mn in Cu migrates toward the top surface of the Cu and reacts with oxygen is a key point for this self-forming barrier process [10] After annealing, MnO_x on the top surface was removed by the two steps, Cu and barrier CMP using conventional slurry. Fig. 2 shows the top view of via Kelvin pattern after CMP. No corrosion or scratches was found. After the CMP, dielectric diffusion barrier SiC_xN_y layer was deposited by plasma-enhanced CVD (PE-CVD) on the Cu. Al pad layer and terminal via were formed for electrical proving and reliability testing.

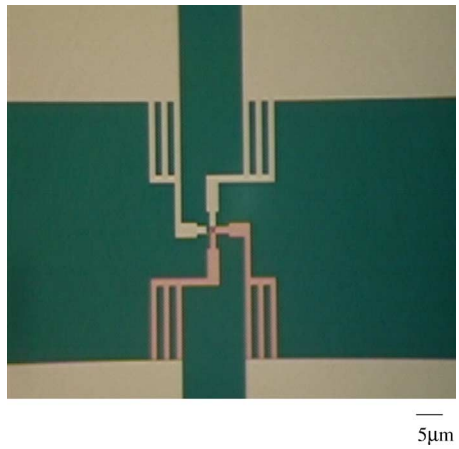

Fig. 2. Top view of the via Kelvin pattern after CMP by optical microscopy.

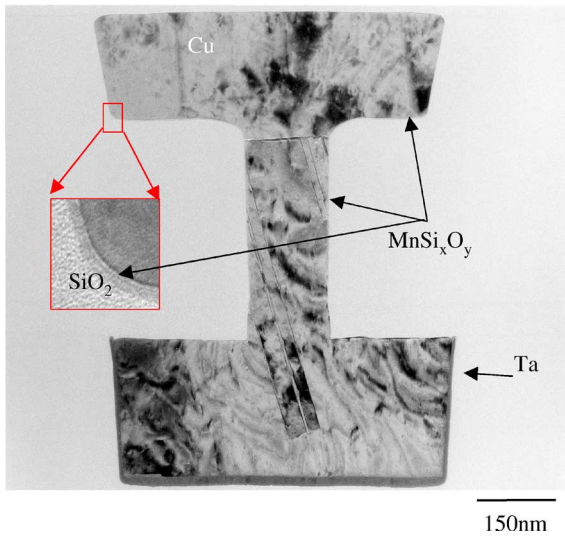

Fig. 3. Cross-sectional TEM images of Cu dual-damascene interconnects with self-formed $MnSi_xO_y$ barrier layer.

III. Results and Discussion

A. Physical Analysis

First of all, physical analysis by transmission electron microscopy (TEM) was carried out to know whether or not self-formed barrier was formed at the interface between Cu and SiO_2 of the trench and via. Fig. 3 shows cross-sectional TEM image of the Cu dual-damascene interconnects with self-formed barrier $MnSi_xO_y$ layer. Looking carefully at the magnified area of the trench bottom, it is found that approximately 2-nm thick and continuous $MnSi_xO_y$ layer was formed at the interface between Cu and SiO_2. No $MnSi_xO_y$ was found at the interface between Cu and SiC_xN_y dielectric diffusion barrier. Another important point found in this image is that no barrier was formed at the via bottom because there was no oxygen at the via bottom during the annealing. Moreover, twin grain lies between lower level interconnect and via. It means that Cu in lower level interconnects and in via completely coalesced during annealing. Fig. 4 shows TEM images of Cu dual-damascene interconnects with conventional PVD Ta. The barrier metal Ta is much thicker than the self-formed $MnSi_xO_y$

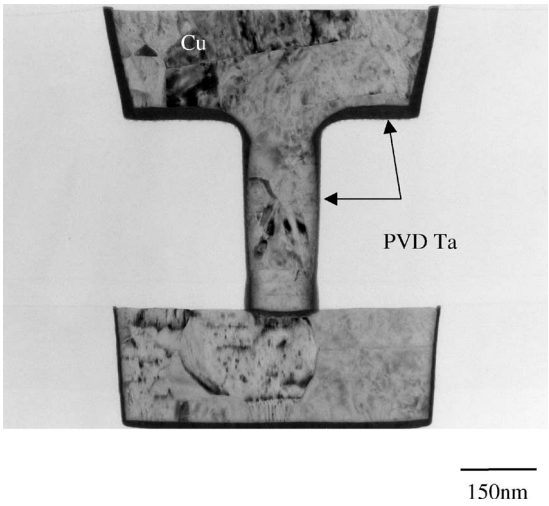

Fig. 4. Cross-sectional TEM image of Cu dual-damascene interconnects with conventional PVD Ta.

barrier layer. PVD Ta barrier exists at the interface as well as at the via bottom. Therefore, the differences between self-formed barrier and conventional PVD Ta were thickness and existence of barrier at via bottom. From these TEM images, via structure with self-formed $MnSi_xO_y$ barrier layer is completely different from that with conventional PVD Ta.

Fig. 5 shows the Mn and Cu electron energy loss spectroscopy (EELS) mapping images of Cu dual-damascene interconnects with self-formed $MnSi_xO_y$ barrier layer. It was also confirmed that continuous Mn layer was at the interface of the via and trench, and that no Mn was in the SiO_2 and Cu. No Cu was found in SiO_2, suggesting that $MnSi_xO_y$ layer has sufficient barrier properties of Cu, and that the concept of self-forming barrier process proposed in [10] works for Cu dual-damascene interconnects.

B. Electrical Characteristics

Leakage current at the intralevel was measured using a comb pattern with the spacing of 0.14 μm and length of 1 m. Actual space was corrected by a scanning electron microscopy (SEM) cross section, and the leakage current was plotted as a function of applied electrical field as shown in Fig. 6. Both samples show usual leakage-current and breakdown behaviors. These facts also suggest that self-formed $MnSi_xO_y$ barrier layer has sufficient barrier properties for Cu. Leakage current of the $MnSi_xO_y$ samples is slightly smaller than in the case of PVD Ta.

The capacitance at intralevel was measured using the comb pattern with the spacing of 0.2, 0.3, and 0.4 μm and is shown in Fig. 7. Basically, no difference was found in either sample. This is probably because, the thickness of $MnSi_xO_y$ layer is so thin compared with the spacing that employed in this measurement.

Via resistance was measured using a chain pattern of 100 000 vias with the diameter of 140 nm, as shown in Fig. 8. First of all, more than 90% yield was obtained for both samples. The criterion of via chain yield is 10 Ω per via. Another important point in Fig. 8 is that the via resistance of $MnSi_xO_y$ was almost half that of conventional PVD Ta. As shown in

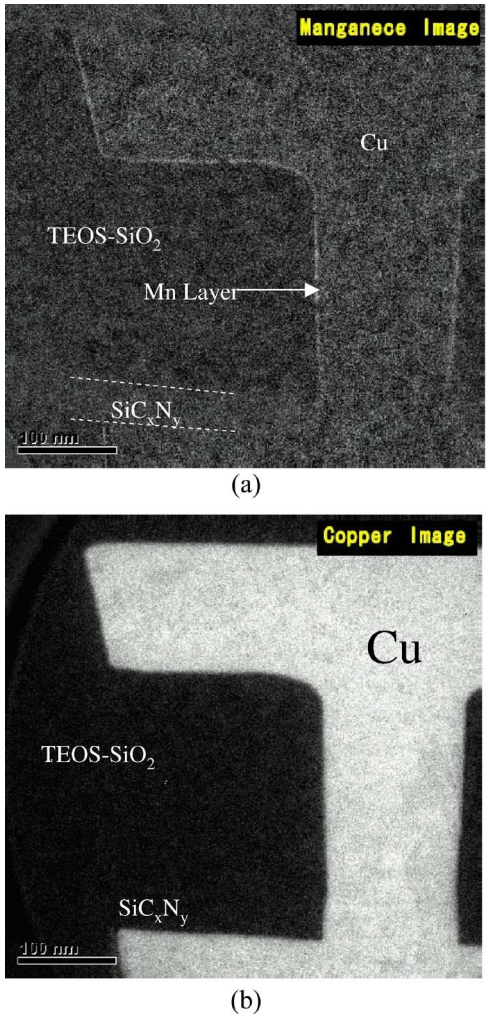

Fig. 5. (a) and (b) are EELS mapping images of Mn and Cu, respectively.

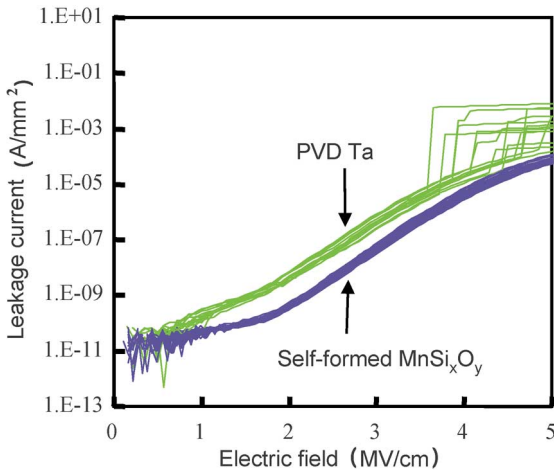

Fig. 6. Leakage current as a function of applied electrical field.

Fig. 4, there is no bottom barrier at the via bottom, which is able to eliminate large resistance of barrier metal Ta and two interfacial resistances of Cu/barrier metal Ta. Therefore, via resistance can be significantly reduced. This fact is consistent with the direct contact via structure, which is formed by sputter etching of barrier metal before Cu seed layer deposition [14].

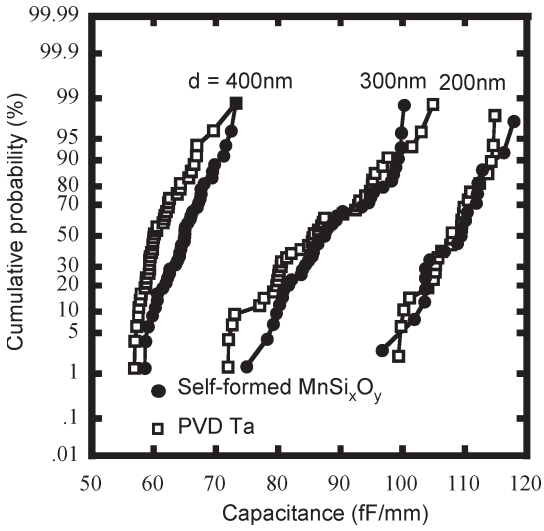

Fig. 7. Distribution of capacitance at intralevel. Spaces were 200, 300, and 400 nm.

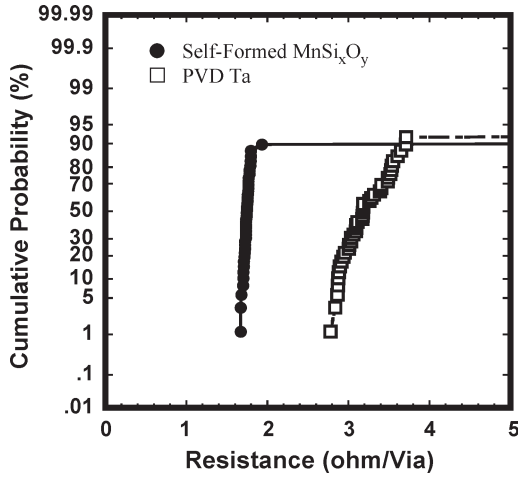

Fig. 8. Distribution of via resistance. Number of the vias is 100 000 and via diameter is 140 nm.

The reduction of via resistance is one of the advantages that this via structure without bottom barrier is able to provide.

C. Reliability Characteristics

SiV measurement was carried out using a via chain with 5-μm wide lower and upper level lines. Diameter and number of vias are 140 nm and 1200, respectively. The testing temperature was 225 °C, which is the most accelerated condition for PVD Ta samples [15]. The failure criterion was 10% relative resistance increase. Fig. 9 shows the relative resistance-increase behavior of PVD Ta as a function of the square root of the testing time.

Many samples failed within 1000-h testing, and abrupt and gradual resistance increases were observed in Fig. 9. Fig. 9 also includes cross-sectional TEM images of SiV testing patterns after testing. The abrupt and gradual relative resistance increase corresponds to the void nucleation under the via and in the via, respectively. Stress-induced void nucleated under the via with abrupt resistance increase is due to there being no electrical redundant layer under the via. On the contrary, the barrier

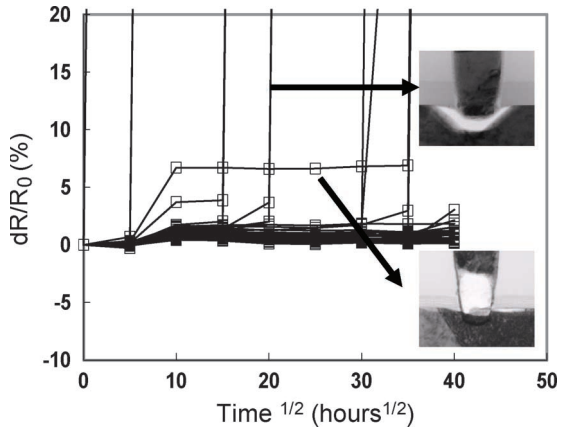

Fig. 9. Relative resistance-increase behavior of PVD Ta samples as a function of square root of the testing time, including cross-sectional TEM images of the SiV pattern after SiV testing.

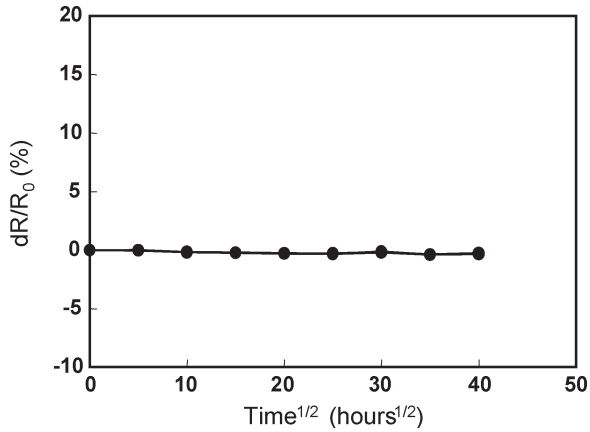

Fig. 10. Relative resistance-increase behavior of self-formed $MnSi_xO_y$ barrier samples as a function of square root of the testing time.

metal Ta barrier served as an electrically redundant layer, which causes a gradual resistance increase when the void nucleated in the via. In both cases, nucleation site of the stress-induced voids must be the Cu/barrier metal Ta interface with the poor adhesion property. Fig. 10 shows the relative resistance-increase behavior of $MnSi_xO_y$ samples during the SiV testing. It is surprising that no sample failed and no resistance increase was observed even after the 1600-h testing. As explained before, $MnSi_xO_y$ samples have no bottom barrier at the via, which means no nucleation site for stress-induced void. In addition, adhesion property at the $MnSi_xO_y$/Cu interface must be good because this $MnSi_xO_y$ layer was formed by a chemical reaction during annealing. This via structure without bottom barrier is able to provide an excellent SiV performance.

SiV performance is also affected by the Cu stress concentration in the via and interconnect trench. The stress concentration in Cu was simulated using the finite element method (FEM). Cu dual-damascene structure is assumed to be free before dielectric diffusion barrier on the top of Cu. The temperature difference was set to be −150 °C from free stress in Cu dual-damascene structure in this simulation. Fig. 11 shows the stress distribution in Cu dual-damascene interconnects with/without 15-nm tantalum (Ta) barrier layer at the via bottom (left and center). It is clearly seen that stress concentration was observed

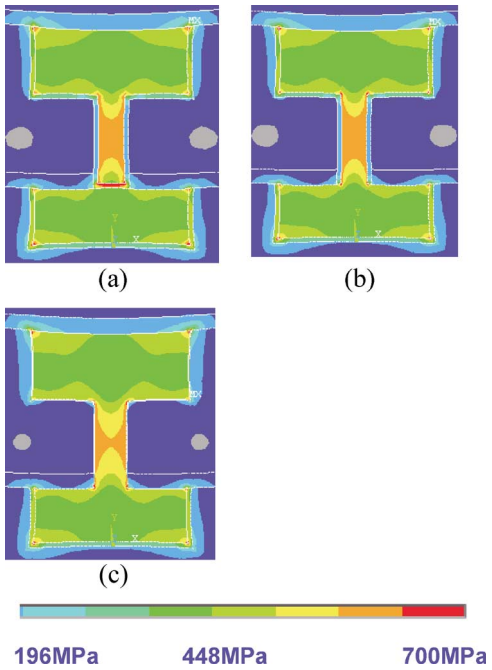

Fig. 11. Simulated stress distribution of Cu dual-damascene interconnects. (a) 15-nm thick barrier layer on the bottom and sidewall of the via and trench. (b) No barrier at the via bottom. The thickness of barrier layer except via bottom is 15 nm. (c) No barrier at the via bottom, either. The thickness of barrier layer except via bottom is 2 nm.

at the bottom barrier [in Fig. 11(a)]. In this simulation, adhesion property at the interface between Cu and Ta could not be included. Therefore, tensile stress concentration occurs in the barrier metal. This stress concentration in barrier metal suggests that the void is easily nucleated at the interface between Cu and barrier metal. On the contrary, only stress concentration at the corner of the via bottom can be found in the case of the via without bottom barrier as shown in Fig. 11(b). In addition, a 2-nm thick barrier metal is able to provide lower stress concentration in the via than in 15-nm thick barrier metal case. From this analysis and discussion, excellent SiV performance of self-formed $MnSi_xO_y$ barrier samples is attribute to no void nucleation site at the via bottom and lower stress concentration around the via bottom as well as in the via, resulting from there being no bottom barrier.

EM testing was carried out using a via EM-testing pattern, which was four-point probable, 100-μm long line with one via at the cathode end of the line. Ten dummy lines were around EM-testing line to monitor the leakage current between testing and dummy lines during the EM testing. The current density and temperature for accelerated condition were 1 MA/cm^2 and 325 °C, respectively. The failure criterion was 10% relative resistance increase, and power supply was stopped at the 20% increase, individually.

Fig. 12 shows the EM cumulative failure distribution for both samples. All PVD Ta samples failed within 200 h, and median time to failure (MTF) and sigma of log-normal distribution for electron-flow direction of M2 upper line through the via to M1 lower line and M1 line through the via to M2 line are 87 h/0.32 and 118 h/0.42, respectively. They are the usual MTF and sigma at this accelerated condition. It is surprising that no self-formed $MnSi_xO_y$ sample for electron-flow direction of M1 line through

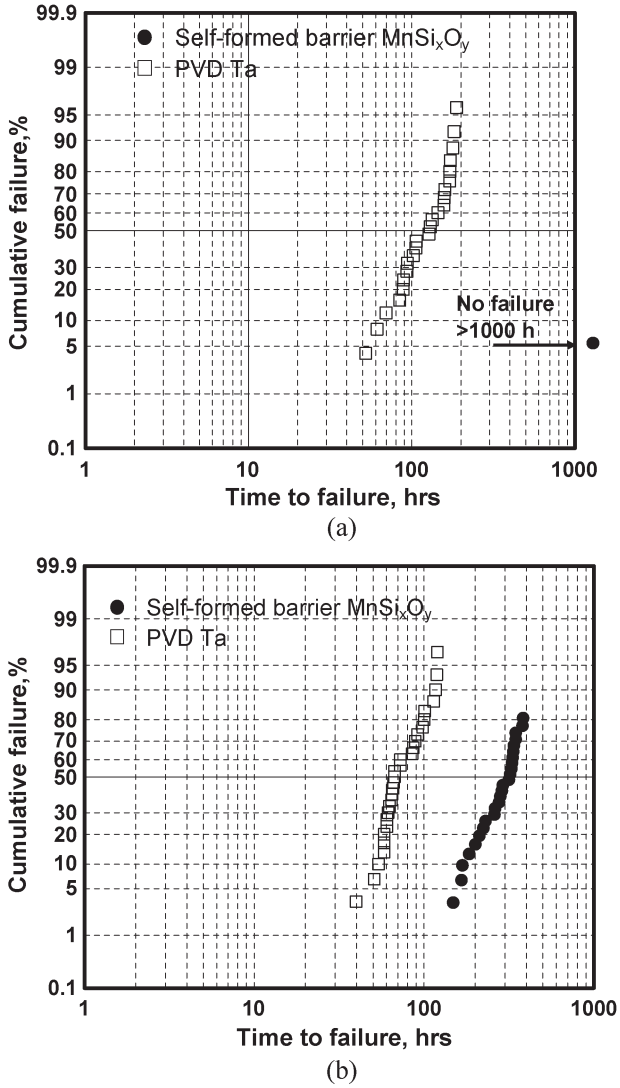

Fig. 12. EM cumulative failure distribution of PVD Ta and self-formed $MnSi_xO_y$ barrier samples. Electron-flow direction of (a) and (b) are from M1 lower line through the via to M2 upper line and M2 line through the via to M1 line, respectively.

the via to M2 line failed even after 1000 h testing. As shown in Fig. 3, via structure without bottom barrier is able to provide continuous Cu atom migration through the via. Therefore, no self-formed barrier $MnSi_xO_y$ sample failed even after 1000-h testing. This fact is consistent with [14]. On the contrary, 80% of self-formed barrier $MnSi_xO_y$ samples for electron-flow direction of M2 line through the via to M1 line failed within 500 h. However, MTF is approximately four times as long as that of PVD Ta sample, suggesting that Cu atom could migrate through the via. In order to know why 80% of samples failed, all samples were checked by an optical microscopy. No void was found in the self-formed $MnSi_xO_y$ barrier sample for electron-flow direction of M1 line through the via to M2 line because no sample failed, as shown in Fig. 12. No void was observed in the PVD Ta sample for electron-flow direction of M2 line through the via to M1 line, either. This is because, M2 power-supply line covers the via and M1 line at the cathode side. Fig. 13 shows the distribution of EM-induced void location from the via. All EM-induced voids in PVD Ta samples were observed within

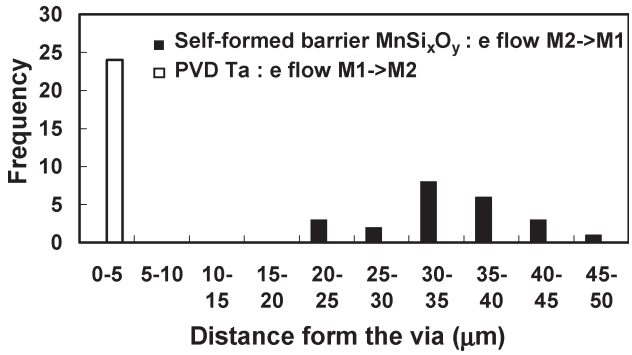

Fig. 13. Distribution of EM-induced void location of PVD Ta and self-formed $MnSi_xO_y$ barrier samples.

5 μm from the via. It is reported that EM-induced void nucleated within the 10 μm from the via, and the number of EM-induced voids decreases with increasing the distance from the via for aluminum (Al) damascene interconnects with flux divergence site of the via [17], [18]. According to tensile stress evolution model by EM of Korhonen *et al.* [19], tensile stress by EM is generated around the flux divergence site of the cathode, EM-induced void nucleates around the flux divergence site in the EM-testing pattern. In the PVD Ta samples, bottom PVD Ta is the flux divergence site for Cu atom migration. Therefore, all EM-induced voids were observed within 5 μm from the via, and their distribution is almost the same as that of Al damascene interconnects [16], [17]. On the other hand, EM-induced voids were observed between 20 and 45 μm from the via. This distribution is completely different from that of self-formed $MnSi_xO_y$ barrier samples. TEM analysis was carried out to confirm the EM-induced void in the line. Fig. 14 shows cross-sectional images of M1 lower level line including EM-induced void (a) and the via (b) after EM testing. No void was found in or around the via, suggesting a continuous Cu atom migration through the via. From this TEM analysis and distribution of EM-induced void, EM perf ormance is not limited by the via structure without bottom barrier. Further investigation is needed to clarify the reason, in which EM-induced void nucleated between 20 and 45 μm from the via for the self-formed barrier samples.

IV. Conclusion

Self-forming barrier process using Cu-2at%Mn seed layer was applied to the Cu dual-damascene interconnects. Approximately 2-nm thick continuous $MnSi_xO_y$ layer was formed at the interface of the Cu and SiO_2 dielectric of the via and interconnect trench. This thin layer is able to provide low leakage current at the intralevel interconnects, meaning that it has a sufficient barrier property for the Cu. From the TEM analysis, no barrier was formed at the bottom of the via because of there being no oxygen at the via bottom. This via structure without bottom barrier provides 50% reduction in via resistance compared with 15-nm PVD Ta samples and excellent reliability performance. In the SiV testing, no failure was found even after 1600 h due to there being no nucleation site of the interface at the via bottom, low stress concentration at the via bottom, and low stress in the via. In the EM testing, no failure was observed for electron-flow direction from M1 lower level line through the via to M2 upper level line after 1000 h because of a continuous Cu atom migration through the via, resulting from there being no bottom barrier of the via. Four times improvement in EM MTF was obtained for the electron-flow direction of M2 upper level line through the via to M1 lower level line. The distribution of EM-induced void location and TEM analysis after EM testing suggest that the EM performance for electron-flow direction from M2 upper level line through the via to M1 lower level line was not limited by the via structure without the bottom barrier.

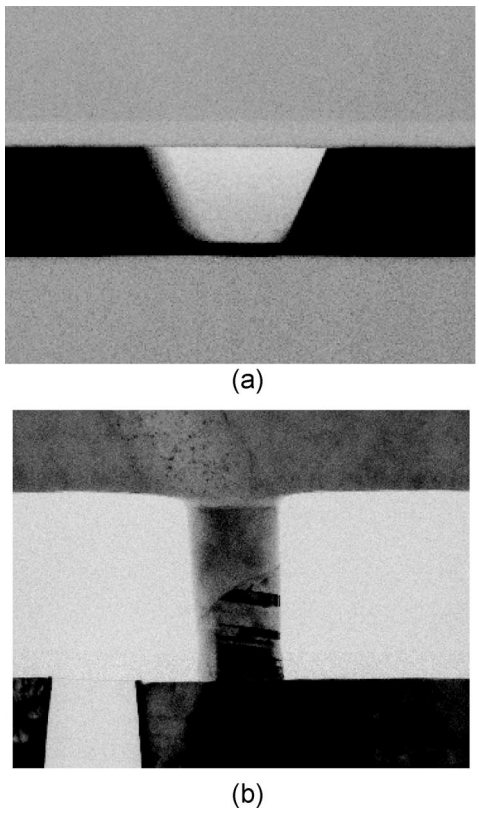

Fig. 14. Cross-sectional TEM images of Cu dual-damascene interconnects with self-formed $MnSi_xO_y$ barrier layer after the EM testing with electron flow of M2 line through the via to M1 line. (a) M1 line including EM-induced void. (b) via without EM-induced void.

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References

[1] A. Kajita, T. Usui, M. Yamada, E. Ogawa, T. Katata, A. Sakata, H. Miyajima, A. Kojima, R. Kanamura, Y. Ohoka, H. Kawashima, K. Tabuchi, K. Nagahata, Y. Kato, T. Hayashi, S. Kadomura, and H. Shibata, "Highly reliable Cu/Low-k dual-Damascene interconnect technology with hybrid (PAE/SiOC) dielectric for 65 nm-node performance eDRAM," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2003, pp. 9–11.

[2] R. Kanamura, Y. Ohoka, M. Fukasawa, K. Tabuchi, K. Nagahata, S. Shibuki, M. Muramatsu, H. Miyajima, T. Usui, A. Kajita, H. Shibata, and S. Kadomura, "Integration of Cu/Low-k dual-Damascene interconnects with a Porous PAE/SiOC hybrid structure for 65 nm-node high performance eDRAM," in *VLSI Symp. Tech. Dig.*, 2003, pp. 107–108.

[3] J. C. Lin, R. Augur, S. L. Shue, C. H. Yu, M. S. Liang, A. Vijayendran, T. Suwwan de Felipe, and M. Danek, "CVD barrier for Cu with nanoporous ultra low-k: Integration and reliability," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2002, pp. 21–23.
[4] C. Prindle, B. Brennan, D. Denning, I. Shahvandi, S. Cuggilla, L. Chen, C. Marcadal, D. Deyo, and U. Bhandary, "CVD TiSiN diffusion barrier integration in sub-130 nm technology nodes," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2002, pp. 182–184.
[5] M. Yamada, S. Omoto, T. Usui, A. Kajita, and H. Shibata, "Stress-induced voiding endurance of Cu-DD interconnects with MO-CVD barrier metal," in *Proc. Jpn. Soc. Appl. Phys., Spring Conf.*, (in Japanese), 2003, p. 823.
[6] C. Bruynseraede, A. H. Fischer, F. Ungar, J. Schumacher, V. Sutcliffe, J. Michelon, and K. Maex, "Comprehensive electromigration studies on dual-Damascene Cu interconnects with ALD WC_xN_y barriers," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2004, pp. 12–14.
[7] K. Higashi, H. Yamaguchi, S. Omoto, A. Sakata, T. Katata, N. Matsunaga, and H. Shibata, "Highly reliable PVD/CVD/PVD stacked barrier metal structure for 45 nm-node Copper dual-Damascene interconnects," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2004, pp. 6–8.
[8] M. Wada and J. Koike, "A new alloying element to copper interconnect for a self-forming barrier layer," in *Proc. Ext. Abstr. 65th Autumn Meet., The Jpn. Soc. Appl. Phys.*, (in Japanese), 2004, p. 711.
[9] ——, "Possibility of self-forming barrier layer by the use of Cu-alloy thin films," in *Proc. Fall Meet. Jpn. Inst. Metals*, (in Japanese), 2004, p. 222.
[10] J. Koike and M. Wada, "Self-forming diffusion barrier of 2-nm thickness in Cu-Mn alloy metallization," *Appl. Phys. Lett.*, vol. 87, p. 041911, 2005.
[11] J. Koike, M. Wada, T. Usui, H. Nasu, S. Takahashi, N. Shimizu, M. Yoshimaru, and H. Shibata, "Self-forming barrier process with Mn addition in Cu metallization," in *Proc. Adv. Metallization Conf., Asian Session*, 2005, pp. 124–125.
[12] T. Usui, H. Nasu, J. Koike, M. Wada, S. Takahashi, N. Shimizu, T. Nishikawa, M. Yoshimaru, and H. Shibata, "Low resistive and highly reliable copper dual-Damascene interconnect technology using self-formed $MnSi_xO_y$ barrier layer," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2005, pp. 246–248.
[13] T. Usui, K. Tsumura, H. Nasu, Y. Hayashi, G. Minamihaba, H. Toyoda, H. Sawada, H. Miyajima, K. Watanabe, M. Shimada, A. Kojima, Y. Uozumi, and H. Shibata, "High performance ultra low-k $(k = 2.0/k_{eff} = 2.4)$/Cu dual-Damascene interconnect technology with Co Cap and self-formed $MnSi_xO_y$ barrier layer for 32 nm-node," in *Proc. IEEE Int. Interconnect Technol. Conf.*, 2006, pp. 216–218.
[14] K. Ueno, M. Suzuki, A. Matsumoto, K. Motoyama, T. Tonegawa, N. Ito, K. Arita, Y. Tsuchiya, T. Wake, A. Kubo, K. Sugai, N. Oda, H. Miyamoto, and S. Saito, "A highly reliability copper dual-Damascene interconnection with direct-contact via structure," in *IEDM Tech. Dig.*, 2000, pp. 265–266.
[15] E. T. Ogawa, J. W. McPherson, J. A. Rosal, K. J. Dickerson, T.-C. Chiu, L. Y. Tsung, M. K. Jain, T. D. Bonifield, J. C. Ondrusek, and W. R. Mckee, in *Proc. IEEE Int. Rel. Phys. Symp.*, 2002, pp. 312–321.
[16] C. K. Hu, L. Gignac, S. G. Malhotra, R. Rosenberg, and S. Boettcher, "Mechanism for very long electromigration lifetime inn dual-damascene Cu interconnections," *Appl. Phys. Lett.*, vol. 78, no. 7, pp. 904–906, Feb. 2001.
[17] T. Usui, T. Watanabe, S. Ito, M. Hasunuma, M. Kawai, and H. Kaneko, "Significant improvement in electromigration of reflow-sputtered Al-0.5wt%Cu/Nb-liner dual-Damascene interconnects with low-k organic SOG dielectric," in *Proc. IEEE Int. Rel. Phys. Symp.*, 1999, pp. 221–227.
[18] T. Usui, T. Watanabe, M. Hatano, S. Ito, J. Wada, and H. Kaneko, "Electromigration of Al-0.5wt%Cu with Nb based liner dual-Damascene interconnects," *Jpn. J. Appl. Phys.*, vol. 43, no. 10, pp. 6957–6962, 2004.
[19] M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, "Stress evolution due to electromigration in confined metal lines," *J. Appl. Phys.*, vol. 73, no. 8, pp. 3790–3799, Apr. 1993.

Takamasa Usui (M'96) received the B.S. and M.S. degrees in metallurgical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1987 and 1989, respectively.

He joined Toshiba Corporation, Kawasaki, Japan, in 1989. Since 2002, he has been with the Center for Semiconductor Research and Development, Toshiba Corporation, where he is engaged in the development of multilevel interconnects for ultralarge scale integration.

Mr. Usui was a recipient of the Best Paper Award from the IEEE International Interconnect Technology Conference 2005. He has been a member of the Electron Device Society since 1993. He is also a member of the Material Research Society.

Hayato Nasu (M'05) received the B.S. degree in electric and electronic engineering from Akita University, Akita, Japan, in 1996.

He joined Toshiba Microelectronics Corporation, Kawasaki, Japan, in 1997. Since 2004, he has been with the Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki, Japan, where he is engaged in the development of multilevel interconnects for ultralarge scale integration.

Mr. Nasu has been a member of the Electron Device Society since 2004.

Shingo Takahashi received the B.S. and M.S. degrees in mechanical sciences and engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1987 and 1989, respectively.

From 1989 to 2000, he was with Kawasaki Steel Corporation, Kawasaki, Japan. In 2000, he joined Sony Corporation, Tokyo, Japan, where he is engaged in process development of advanced copper/low-k interconnects for ultralarge scale integration.

Noriyoshi Shimizu received the M.S. degree in materials science from Tokyo Institute of Technology, Tokyo, Japan.

Since 1998, he has been a Senior Researcher with Fujitsu Laboratories, Kawasaki, Japan, where he works on Cu interconnects research and is in charge of the electroplating technology for fabricating dual damascene Cu interconnects, development of device reliability analysis techniques, and physical vapor deposition technology development. He has published more than 40 technical papers and holds 63 patents.

Mr. Shimizu is a member of the Advanced Metallization Conference Committee and the Japan Applied Physics Society.

T. Nishikawa, photograph and biography not available at the time of publication.

Masaki Yoshimaru (M'05) was born in Ooita, Japan, in 1951. He received the B.S. and Ph.D. degrees in electronic engineering from Kyushu University, Fukuoka, Japan, in 1975 and 2002, respectively.

In 1975, he joined Oki electric industry Co., Ltd., Tokyo, Japan, where he was engaged in research and development on the very large scale integration process technology. Since 2004, he has been working for a joint research between universities and the industry with the Semiconductor Technology Academic Research Center, Yokohama, Japan.

Dr. Yoshimaru is a member of the Japan Society of Applied Physics and the Electron Devices Society.

Hideki Shibata received the B.S. degree in metallurgical engineering and the Ph.D. degree in electrical and computer engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1982 and 1995, respectively.

In 1982, he joined the Semiconductor Device Engineering Laboratory, Toshiba Corporation, Kawasaki, Japan. Since 1995, he has been engaged in the development of advanced copper/low-k interconnects integration technology for high-performance logic devices. He is currently the Senior Manager with Advanced BEOL Technology Department, Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki, Japan.

Dr. Shibata is a member of the Electron Device Society and the Japan Society of Applied Physics.

Makoto Wada received the B.S., M.S., and Ph.D. degrees in materials science from Tohoku University, Sendai, Japan, in 2000, 2002, and 2005, respectively. His Ph.D. dissertation was on the self-forming barrier layer process with Cu-Mn alloy metallization.

In 2005, he joined the Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki, Japan, where he is engaged in the development of the multilevel interconnects for semiconductor devices and related material processing.

Dr. Wada is a member of the Japan Society of Applied Physics and the Material Research Society.

Junichi Koike received the B.S. and M.S. degrees in metallurgical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1983 and 1985, respectively, and the Ph.D. degree in materials science from Northwestern University, Evanston, IL, in 1989.

He was a Director's Postdoctoral Fellow with Los Alamos National Laboratory in 1989–1991, and an Assistant Professor with Oregon State University, Carvallis, OR, in 1991–1994. He joined the Department of Materials Science, Tohoku University, Sendai, Japan, in 1994, as an Associate Professor and became a Full Professor in 2005. His main research topics are the study of microstructure-reliability relation in Cu interconnect and the development of electrode materials for advanced electronic devices. He presented a numerous number of invited talks on these subjects at international conferences.

Dr. Koike is a member of the Materials Research Society and TMS.