Three-Dimensional Integration Technology for Real Time Micro-Vision System

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Abstract

It becomes possible to achieve the real time micro-vision system with extremely high image processing speed if three-dimensional LSI comes into reality because a higher level of parallel processing can be performed in three-dimensional LSI. Then, we have proposed a new three-dimensional integration technology for such real time micro-vision system with high image processing speed. Several key technologies for three-dimensional integration such as formation of buried interconnection and micro-bump, wafer thinning, wafer alignment and wafer bonding have been developed.

1. Introduction

Recently, the demand to very fast image processing LSI with real time operation capability has rapidly increased [1]. However, it is very difficult to achieve such LSI by using a conventional two-dimensional (2D) LSI technology because the eventual image processing speed is limited by converting 2D image data array to 1D image data stream. Long interconnections required in 2D image processing LSI also limit the processing speed. These problems can be solved if three-dimensional (3D) LSI technology can be used for fabricating the image processing LSI because 2D image data can be treated as it is and we can use many short interconnections in the vertical direction which dramatically reduce a wiring delay. In the past, many researchers tried to develop 3D LSI technology using laser annealing technique, zone melting technique, solid phase epitaxial technique and so

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on[2][3]. However, such 3D LSI technology had not been employed in production because it was very complicated and expensive technology. In this research, we propose more realistic 3D LSI technology based on a wafer bonding technique using micro-bumps and describe the real time micro-vision system with 3D LSI structure.

2. Configuration of Micro-Vision System

Figure 1 represents a basic configuration of 3D image processing LSI for the real time micro-vision system which consists of four layers of image sensor array layer, amplifier and AD converter array layer, data latch and masking circuit layer and processor array and output circuit layer [4]-[7]. Each layer is connected vertically using high density of vertical interconnections. Therefore, 2D image signals are simultaneously transferred in the vertical direction and processed in parallel in each LSI layer. As a result, the dramatic improvement of the processing speed can be expected by using 3D image processing LSI.

The 3D image processing test circuits for the edge detection using Laplacian operator were designed. One image frame was divided to many processing units which can be operated in parallel. Eight by eight pixels, one amplifier and AD converter, a block of data latches and one ALU are accommodated in one processing unit as shown in Fig. 2. Although it is hopeful that one ALU and one AD converter are accommodated in one pixel, it is very difficult since the pixel area is too small to do it. As a result, in the case of VGA with 640x480 pixels, 80x60 processing units become to operate in parallel. To guarantee the continuity in image processing between two adjacent processing units, the processing unit has four overlapping parts in its verge as shown in Fig. 3. The signal data are processed sequentially within each processing unit. However, the very fast pipeline processes are employed in each processing unit in order to accelerate the processing speed as shown in Fig. 4. Two-stage pipeline operation is performed in this 3D LSI. The first stage is the photodetector, the amplifier and the AD converter. The second stage is the shift register and the ALU. Thus, a very high performance can be achieved in this 3D image processing LSI by combining the parallel processing and the high speed pipeline operation. Figures 5 and 6 show the block diagram of the processing unit and a part of timing chart, respectively.

3. Three-Dimensional LSI Fabrication process

The cross-sectional view of 3D image processing LSI is shown in Fig. 7 where the top

layer for image sensor array is omitted. This 3D LSI is fabricated by stacking several thinned LSI wafers on the thick Si wafer. The wafers are glued by the adhesive layer which is formed between two wafers. The electrical connections between the upper and lower layers are achieved through the buried interconnections and micro-bumps. The buried interconnections in the thinned LSI wafer are formed by poly-Si or CVD W while those in the thick Si wafer formed by electroplated Cu. In/Au evaporated in vacuum is used as the micro-bump in the thinned LSI wafer while electroplated Cu is used as the metal bumps in the thick Si wafer. The Cu bumps which are formed in the back side of the thick Si wafer are used to bond such 3D LSI chip with the image sensor array on its surface onto the substrates of the package or the multi-chip module (MCM).

The process sequence to fabricate such 3D LSI is shown in Fig. 8. In the figure, the sequence to form the Cu buried interconnections and the Cu bumps in the thick Si wafer are omitted. The 2D LSI wafer with buried interconnections which act as vertical interconnection is used as a starting wafer for 3D LSI. The buried interconnections are formed by depositing n^+poly-Si or CVD W into trench which is formed through the field oxide. Such 2D LSI wafer with buried interconnections are glued to a quartz glass and thinned from the back side to around 30μm by grinding and chemical-mechanical polishing (CMP). The thinned wafer is bonded to the thick Si wafer through the micro-bumps after careful wafer alignment. The adhesive layer with thickness of 1μm is inserted between two wafers to enhance the bondability of two wafers. The 3D LSI can be fabricated by repeating such sequence.

The Cu bumps are formed in the back side of the thick Si wafer in order to obtain many output pins. In packaging of this 3D image processing LSI chip, the conventional bonding technique such as flip-chip bonding cannot be used because this chip has the image sensor layer on the top surface. Therefore, it is necessary to form the Cu buried interconnections and the Cu bumps in the thick Si wafer which is the bottom substrate of 3D LSI. The Cu buried interconnections are formed by trench-etching through the thick Si wafer followed by electroplating to bury Cu into the trenches.

4. Development of Key Technologies for Three-Dimensional LSI

Formation of buried interconnection and micro-bump, wafer thinning, wafer alignment and wafer bonding are key technologies for achieving our 3D LSI. Then, these key tech-

nologies have been developed and the device characteristics on the stacked wafer have been evaluated. It is required to form the deep Si trenches in order to form the buried interconnections in the thinned LSI wafer and the thick Si wafer. The Si trench with the depth of around 30μm in the thinned LSI wafer was formed using ICP (Inductively Coupled Plasma) etching with mixed gas of SF_6 and O_2 as etching gas. The wafer was cooled to avoid the temperature rise during etching. The experimental results are shown in Fig.9 where the etching depth and the etching rate of Si trench are plotted versus the trench size. It is obvious in the figure that a Si trench with the depth of more than 30μm can be formed by ICP etching with mixed gas of SF_6 and O_2 although the trench depth decreases as the trench size is reduced due to the micro-loading effect. Finally the Si trench with the size of 2μm X 2μm and the depth of 30μm is used for the buried interconnection in the thinned LSI wafer. The Si trench should be oxidized and filled with n^+poly-Si or CVD W to form the buried interconnection. Figure 10 showd the SEM cross-section of the oxidized Si trench filled with n+poly-Si. The Si trench with the depth of more than 100μm has to be formed for the buried interconnection in the thick Si wafer because the final thickness of the thick Si wafer is more than 100μm. The mixed gas of SF_6 and carbon fluoride was used to form such deep Si trench. The SEM cross-section of the deep Si trench with the depth of around 100μm is shown in Fig.11. It is clear from the figure that the deep Si trench with the depth of around 100μm can be formed by using ICP etching with mixed gas of SF_6 and carbon fluoride.

Grinding and chemical-mechanical polishing (CMP) techniques were used to thin the wafer to 30μm. We did not thin the wafer less than 30μm to avoid wafer cracking during handling although is was easy to thin to less than 30μm. Wafer thickness variation after thinning was very small as 30μm$\pm$0.5μm in six inch wafer as shown in Fig.12. A photograph taken from the back side after thinning the wafer to 30μm only by grinding is shown in Fig.13 where the line and space patterns of trench are exposed. For a wafer alignment, we have developed a new 3D wafer aligner as shown in Fig.14. The wafer stage can be precisely controlled with accuracy of 50nm in x, y, z direction by piezo actuators in this aligner. The six inch wafers can be aligned with the alignment tolerance of $\pm$1μm. We can detect the infrared light signal for alignment which has passed through ten Si layers including the thick Si wafer. The gap between two wafers is monitored in-situ

using the gap sensors and precisely controlled during alignment. This aligner can also supply a mechanical pressure to the wafer during bonding in order to firmly contact the micro-bumps in the upper and lower wafers each other and to glue these wafers. The mechanical pressure is also monitored in-situ using the load sensor so as to supply the very uniform mechanical pressure. The pattern alignment between the upper thinned wafer and the lower thick wafer using 3D wafer aligner is demonstrated in Fig.15. Both patterns in the upper wafer and the lower wafer are clearly observed in the figure.

In/Au micro-bumps and epoxy adhesive layer were used to bond two wafers. Figure 16 shows the SEM micrograph of via hole for the micro-bump which is formed through the photo-resist and the polyimide film using O_2 RIE (Reactive Ion Etching) before forming In/Au micro-bumps. The photo-resist is used for the lift-off and the polyimide for the planarization. The process sequence to form the via hole and the In/Au micro-bump is shown in Fig.17. The photomicrograph and SEM micrograph of the micro-bumps formed by the lift-off technique are shown in Figs.18 and 19. As is obvious from figures, we could fabricate good In/Au micro-bumps although the shape of 5μmX5μm micro-bumps was slightly deformed. In order to confirm the good electrical contact between the micro-bumps in the upper wafer and the lower wafer, the test structure as shown in Fig.20 was fabricated. It was confirmed that the good electrical contact is obtained between two micro-bumps after bonding by optimizing the process conditions for the micro-bump and wafer bonding as shown in Table 1. The contact resistance between two micro-bumps was around 3 ohm.

Figure 21 shows SEM micrograph of electroplated Cu bumps formed on the thick Si wafer. In order to mount the 3D image processing LSI with such Cu bumps onto the substrate of the package or the multi-chip module (MCM), it is necessary to form Ag filled epoxy adhesive only on the surface of the Cu bumps to prevent electrical short. We have newly developed the printing method as shown in Fig.22. The photograph of the Cu bumps with the Ag filled epoxy adhesive formed on their surface using this method is shown in Fig.23. It is clear from the figure that the Ag filled epoxy adhesive is formed only on the surface of the Cu bumps. SEM micrograph of LSI chip mounted on the MCM substrate using the printing method is shown in Fig.24. As is clear in the figure, it was confirmed that the LSI chip with the Cu bumps on the back side can be easily mounted

onto the MCM substrate by using the printing method. In the test module shown in Fig.24, Al wirings are also formed on the back side of LSI chip so as to connect the Cu bumps. Therefore, the contact resistance of Cu bumps can be measured. Consequently, a relatively low contact resistance of around 10 ohm per one Cu bump is obtained at present although it should be reduced more.

The device characteristics of MOS transistors in the thinned Si wafer which is stacked on the thick Si wafer have been evaluated. As a result, relatively good characteristics were obtained as shown in Fig.25.

5. Summary

A new 3D integration technology to achieve the real time micro-vision system with extremely high image processing speed has been proposed. A basic configuration of such real time micro-vision system was also described. In addition, several key technologies for three-dimensional integration such as formation of buried interconnection and micro-bump, wafer thinning, wafer alignment and wafer bonding have been developed. We have succeeded to form the deep Si trenches for the buried interconnections by using ICP (Inductively Coupled Plasma) etching. Furthermore, we have developed a special wafer aligner for three-dimensional integration. It was also demonstrated that relatively good characteristics are obtained in MOS transistors formed in a thinned Si wafer which is stacked on the thick Si wafer.

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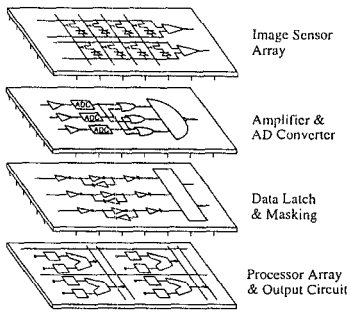


Fig.1 Real time micro-vision system with 3D structure.

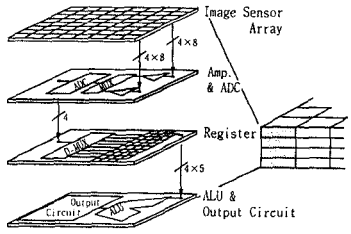


Fig.2 Description of processing unit of real time micro-vision system.

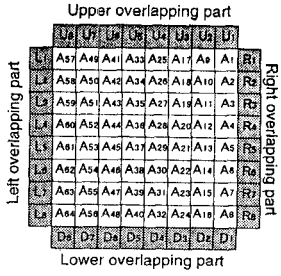


Fig.3 Processing unit with 4 overlapping parts.

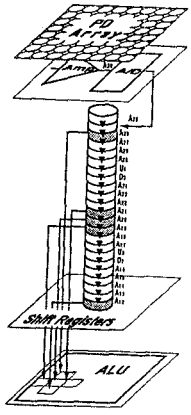


Fig.4 Data flow in the pipeline processing unit.

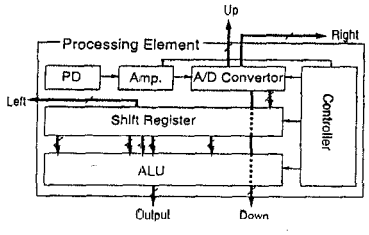


Fig.5 Block diagram of the processing unit.

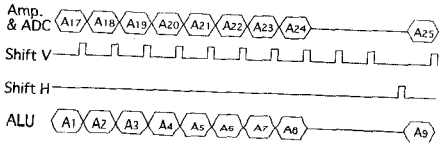


Fig.6 Timing chart in the processing unit.

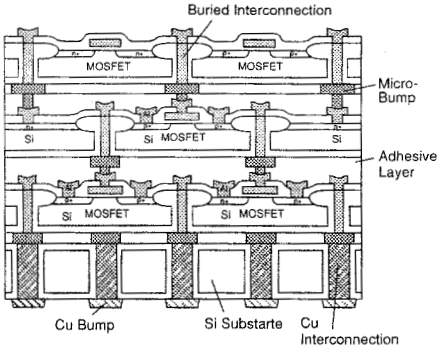


Fig.7 Cross-sectional view of 3D image processing LSI.

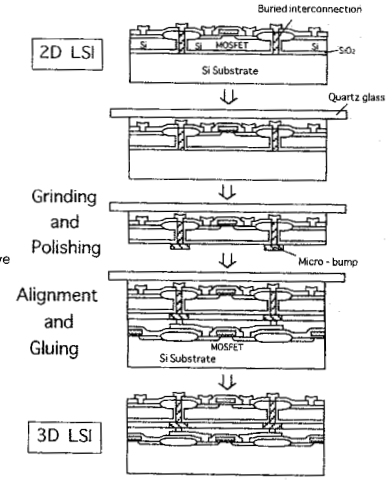


Fig.8 Fabrication sequence of 3D LSI.

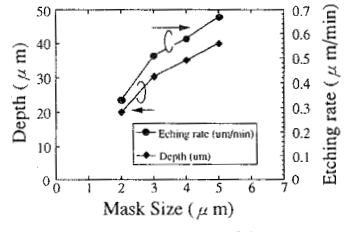


Fig.9 Trench depth and etching rate as a function of trench size.

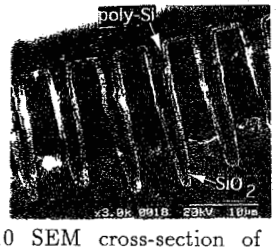


Fig.10 SEM cross-section of oxidized deep trench filled with poly-Si.

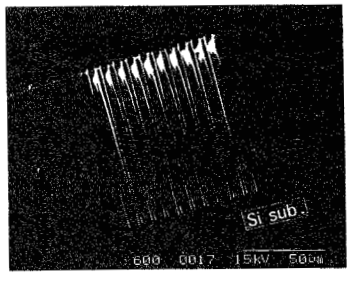


Fig.11 SEM cross-section of deep silicon trench. (width=5μm, depth=100μm)

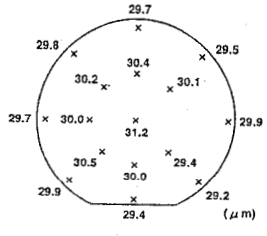


Fig.12 Thickness variation in 6 inch wafer after thinning.

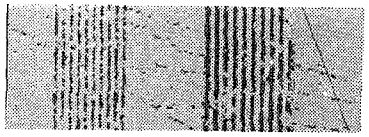


Fig.13 Photomicrograph of the back surface of silicon wafer after grinding.

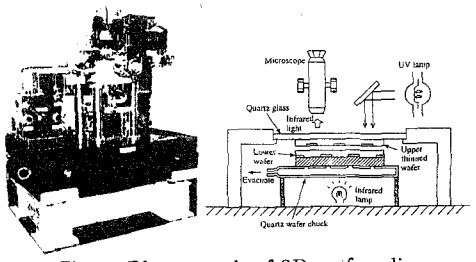
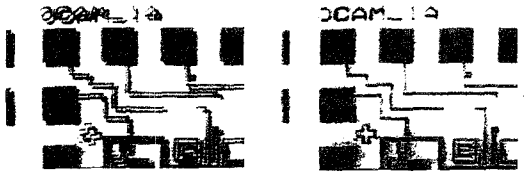


Fig.14 Photograph of 3D wafer aligner.



(a) before alignment (b) after alignment

Fig.15 Wafer alignment using 3D wafer aligner.

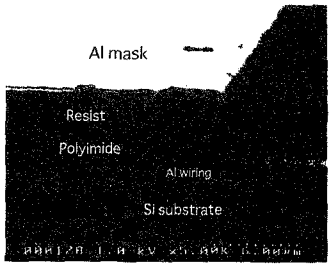


Fig.16 SEM micrograph of via hole formed by O_2-RIE before In/Au deposition.

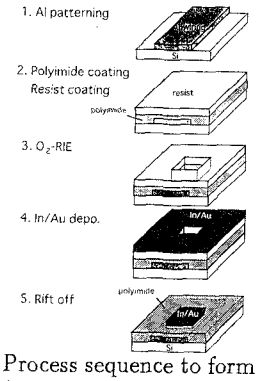


Fig.17 Process sequence to form via hole and In/Au mico-bump.

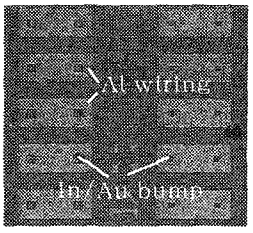
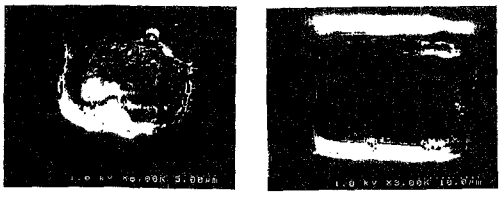


Fig.18 Photomicrograph of In/Au micro-bumps.



(a) 5μm x 5μm In/Au (b) 20μm x 20μm In/Au

Fig.19 SEM micrograph of In/Au micro-bump.

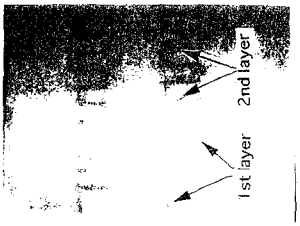


Fig.20 Photomicrograph of test structure to evaluate the contact resistance between micro-bumps.

		A	B	C	D	E	F
Bump Thickness Au / In (nm / nm)	Upper Bump	100/900	100/900	500/500	500/500	100/900	100/900
	Lower Bump	100/900	100/900	500/500	500/500	500/500	500/500
Soldering Temperature(℃)		150	90	90	150	150	150
Soldering Time (minute)		1	30	30	5	5	1
Contact Resistance		○	○	×	×	○	○

Table 1 Evaluation results of micro-bump contact resistance.

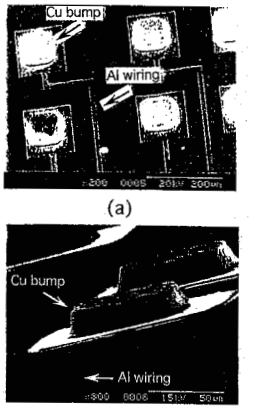


Fig.21 SEM micrograph of electroplated Cu bumps.

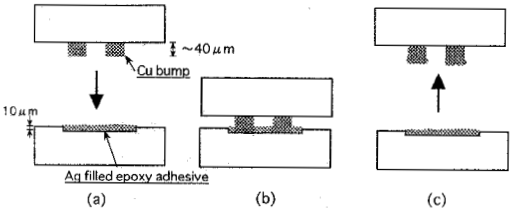
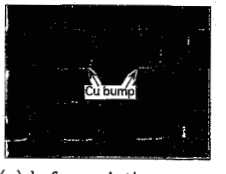


Fig.22 Printing process sequence to form Ag filled epoxy adhesive on Cu bumps.



(a) before printing

(b) after printing

Fig.23 Plane view of Cu bumps before and after printing Ag filled epoxy adhesive.

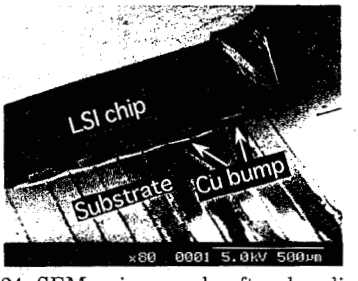


Fig.24 SEM micrograph after bonding LSI chip.

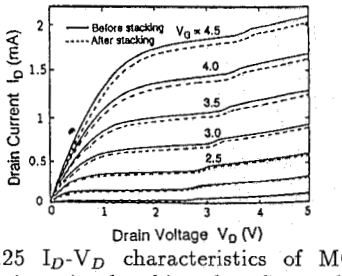


Fig.25 I_D-V_D characteristics of MOS transistor in the thinned wafer stacked on the thick wafer.