40-Gb/s IC's for Future Lightwave Communications Systems

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***Abstract*—This paper describes the device, circuit design, and packaging technologies applicable to 40-Gb/s-class future lightwave communications systems. A 0.1-μm gate InAlAs/InGa-As high electron mobility transistors (HEMT's) with InP recess etch stopper was adopted mainly for IC fabrication. Fabricated IC's demonstrate excellent data-multiplexing, demultiplexing, and amplifying operation at 40 Gb/s.**

***Index Terms*—Demultiplexing, distributed amplifiers, flip-flops, MODFET integrated circuits, multiplexing, optical fiber communication.**

I. Introduction

THERE is an urgent need to expand transmission capacity because of the movement toward broadband integrated services digital network (ISDN) and multimedia services. Capacity will surely increase to terabits per second in the next century. At present, electrical time-division multiplexing and demultiplexing (ETDM), is the most mature system. Systems of 10 Gb/s are about to be brought into commercial use [1]. The record bit rate now exceeds 20 Gb/s/channel [2]. With the emergence of wavelength-division-multiplexing (WDM) technology, total transmission throughput has dramatically increased to beyond 1 Tb/s with 55 [3] and 132 [4] WDM channels. However, it is also true that the development of practical, dense WDM systems requires further technological advances in photonic components. Meanwhile, optical time division multiplexing (OTDM) systems are potential candidates for overcoming current performance limits [5], [6]. However, their applicability to commercial-level systems has yet to be studied.

In terms of system practicality, reliability, and cost, we still have to improve the speed of electronic IC's to around 40 Gb/s and more even though WDM and OTDM technologies relax the demands on the single-channel bit rate. Recently, several 40-Gb/s class IC's have been developed by using GaAs heterojunction bipolar transistors (HBT's) [7]–[9] and Si bipolar transistors [10], [11]. A 50-Gb/s Si bipolar multiplexer (MUX) [10] is an excellent result because of its relatively low transistor speed. But, a 40-Gb/s amplifier is really difficult to make with Si bipolars. Even if we put decision circuits aside, no single process is yet able to cover all the key components.

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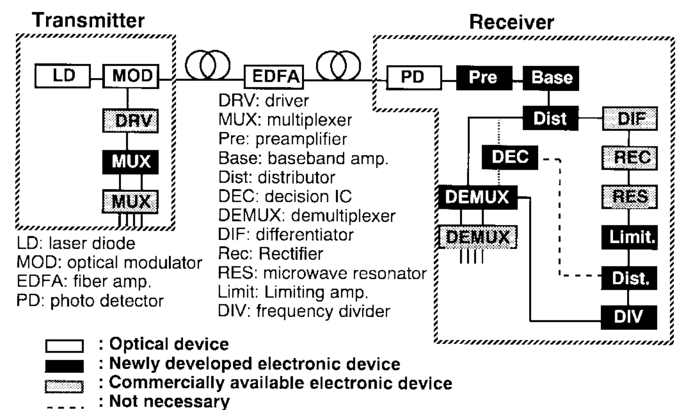

Fig. 1. Basic transmitter and receiver configuration for lightwave communications systems.

This paper describes novel 40-Gb/s class analog and digital IC technologies along with their packaging technology for future lightwave communications systems. A 0.1-μm gate InP-based high electron mobility transistor (HEMT) is mainly used for IC fabrication. In combination with high-speed, mature device technology and advanced circuit/package design technology, all the key components in the transmitter and the receiver achieve 40-Gb/s operation.

II. Requirements for Optical Communication IC's

Fig. 1 depicts the basic transmitter and receiver configuration for lightwave communications systems. The functionality required for transmitter and receiver electronic IC's is basically the same (multiplexing, amplifying, retiming, regenerating, and demultiplexing) for all TDM and WDM transmission systems with the small exception of extra blocks (e.g., exclusive-OR or wideband mixer) for coherent systems. The transmitter block consists of a laser diode (LD), an optical modulator (MOD), a modulator driver (DRV), and multiplexers (MUX's). The receiver block consists of a photodiode (PD), a preamplifier (Pre), a baseband amplifier (Base), a decision circuit (DEC), demultiplexers (DEMUX's), and a clock recovery circuit that includes a differentiator (DIF), a rectifier (REC), a resonator (RES), and a limiting amplifier (Limit). The transmitter and receiver IC's, except for the clock recovery block, require broadband operation from near dc to the maximum bit rate with good eye openings.

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TABLE I
LISTS OF OUR HIGH-END FRONT-END IC'S FOR HIGH-SPEED LIGHTWAVE COMMUNICATIONS SYSTEMS

Circuit, Ref.	Bandwidth/ Bit rate	Gain	Output	Power	Device / Gate length
2:1 Multiplexer, [24]	46 Gbit/s	- - -	1.2 Vpp	1.7 W	InP HEMT / 0.1 μm
Preamp., [17]	DC - 32 GHz	9 dB	1.0 Vpp	440 mW	InP HEMT / 0.1 μm
Baseband amp., [19]	DC - 47 GHz	16 dB	1.2 Vpp	1.1 W	InP HEMT / 0.1 μm
Sig. distributor, [22]	DC - 100 GHz	-2.5 dB	0.5 Vpp	1.1 W	InP HEMT / 0.1 μm
Decision, [27]	8 - 24 Gbit/s	- - -	1.2 Vpp	1.8 W	GaAs MESFET / 0.2 μm
1:2 Demultiplexer, [24]	1 - 40 Gbit/s	- - -	1.2 Vpp	1.9 W	InP HEMT / 0.1 μm
Freq. divider, [16]	DC - 40.4 GHz	- - -	0.4 Vpp	550 mW	InP HEMT / 0.1 μm
Limiting amp., [17]	34 - 40 GHz	17 dB	10 dBm	70 mW	InP HEMT / 0.1 μm

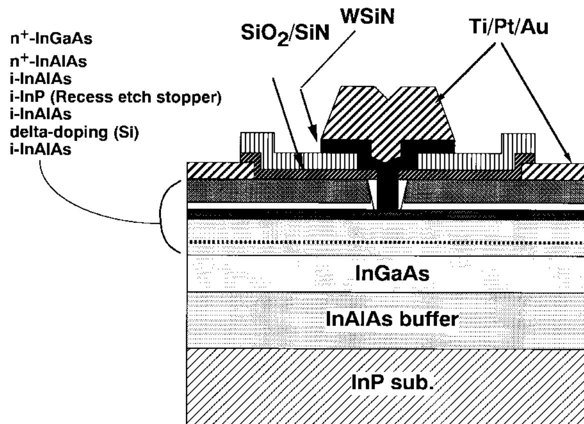

Fig. 2. Schematic of 0.1-μm gate InAlAs/InGaAs/InP HEMT.

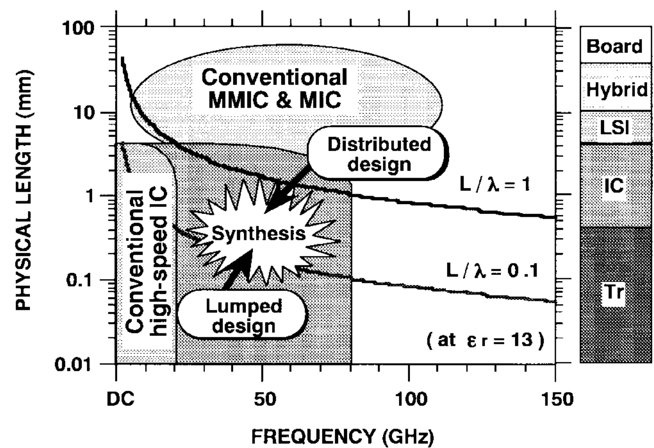

Fig. 3. Ratio of physical length to wavelength for GaAs devices. It also shows the concept for ultra-broadband analog IC design.

III. DEVICE

For the device technology, InP-based HEMT's and HBT's are considered to be the best candidates for 40-Gb/s applications in terms of their speed performance [12], [13]. AlGaAs/GaAs HBT's [14] and 0.1-μm-class GaAs MESFET's [15] are the next best because of their relatively lower speed, but much greater maturity. A 0.1-μm gate InAlAs/InGaAs HEMT [16] was adopted mainly for IC fabrication in this paper. Fig. 2 shows a schematic of the HEMT structure. We developed nonalloyed ohmic contacts using n^+-InGaAs/n^+-InAlAs layers and a T-shaped gate with a 0.1-μm footprint to reduce the parasitic resistances. We also inserted a thin InP layer in the InAlAs barrier as a recess etch stopper. It greatly improved the threshold voltage uniformity because it enables the precise control of the barrier thickness. The average threshold voltage was -0.5 V and the standard deviation was less than 40 mV in a 2-in wafer. The average f_T, $f_{\max}$, and transconductance were 169 GHz, 264 GHz, and 1.0 S/mm, respectively. Moreover, low-loss pn-junction level-shift diodes were integrated instead of Schottky diodes using HEMT's, which reduced the turn-on resistance by a factor of two, resulting in faster circuit operation.

IV. CIRCUIT DESIGN

Table I summarizes the function blocks and corresponding performances of the electronic IC's we developed. All the analog and digital IC's, except the decision IC, achieved 40-Gb/s operation. In this section, we discuss the circuit design technologies along with several IC fabrication results using InP HEMT's. We also describe the IC's using GaAs MESFET's for some cases.

A. Analog IC's

Fig. 3 shows the ratio of the physical length to the wavelength for GaAs devices. As data rates increase beyond 10 Gb/s, the wavelength of the signal approaches the physical size of IC chips, which gives rise to substantial difficulties in designing broadband IC's: 1) numerous parasitics, 2) cavity resonance, and 3) bandwidth limitation due to lumped-circuit treatment. Another difficulty is the requirement of broad-bandwidth operation from dc to the maximum bit rate. These are the major reasons that transistor performance no longer directly reflects the circuit and module performance.

One approach to overcoming the performance limit is the synthesis of distributed and lumped-circuit design techniques. Fig. 4 shows the basic circuit diagram of our distributed amplifier for use in baseband operation [18]. Distributed amplifiers are commonly used in millimeter wave applications. Their great merit is that they can significantly widen the bandwidth. Each unit is a simple, small-sized cascode amplifier. The parasitic capacitance of FET's is effectively utilized as a circuit element to enable velocity-matched signal transmission between the gate input and drain output lines. However, we run into a serious problem when we try to apply this design to baseband amplifiers; namely, the drain conductance

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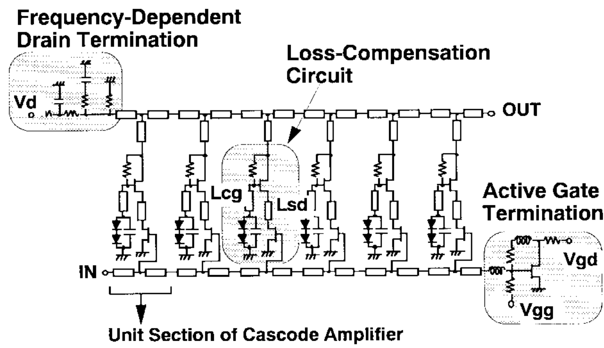
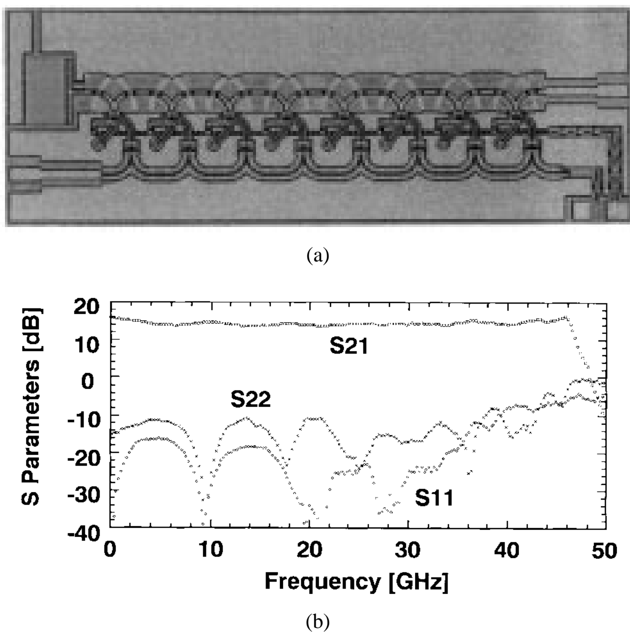


Fig. 4. Basic circuit diagram of distributed amplifier for broadband application.



(a)

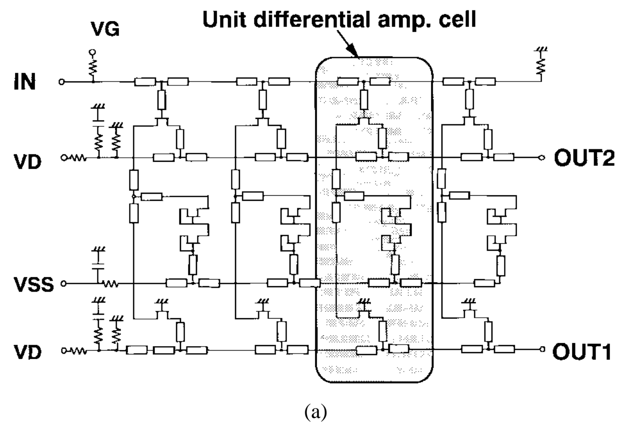
(b)

Fig. 5. (a) 16-dB gain, dc-to-47-GHz baseband amplifier chip microphoto and (b) measured S parameters.

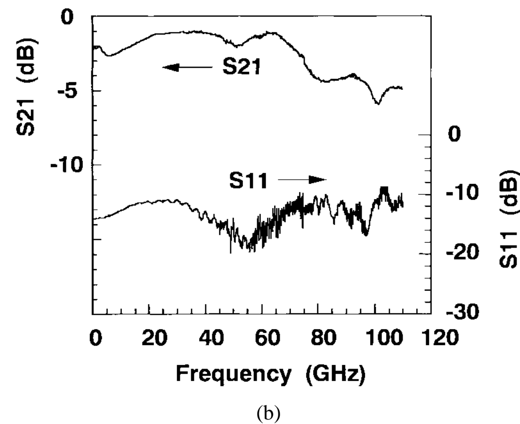
of the FET's degrades the dc gain. To cope with this, a novel frequency-dependent bias termination was devised to compensate for the dc gain. Another wideband design we devised is the loss compensation circuit. The two additional transmission lines $(L_{\rm cg}, L_{\rm sd})$ inserted here act as inductors to increase the negative resistance and thereby compensate for the loss at high frequencies. The active gate termination improves the noise figure at low frequencies.

A typical example is a dc-to-47-GHz, 16-dB distributed baseband amplifier IC using 0.1-μm gate InP HEMT's [19]. The chip microphoto and its performance are shown in Fig. 5. The IC consumes 1.1 W. Its excellent gain-bandwidth product of 297 GHz owes to the loss-compensation circuit. We designed several baseband amplifier IC's with different gain-bandwidth specs [20], [21].

Another example of the distributed design is a dc-to-100-GHz 1 : 2 signal distributor IC using the 0.1-μm-gate HEMT's [22]. The circuit diagram and its performance are shown in Fig. 6. One feature of the circuit design is the application of a distributed amplification technique to



(a)



(b)

Fig. 6. (a) DC-to-100-GHz, 1 : 2 signal distributor circuit diagram and (b) measured S parameters.

a differential circuit to enhance wideband performance. Conversion loss between the input and each output port is less than 2.5 dB below 70 GHz and less than 5 dB over the bandwidth. Another trial of distributed nonlinear baseband circuit is a dc-to-38-GHz distributed analog multiplier using the InP HEMT's [23].

B. Digital IC's

High-speed multiplexer (MUX) and demultiplexer (DEMUX) IC's are key digital elements in transmitter and receiver hardware. We developed a 46-Gb/s 2 : 1 multiplexer IC and a 40-Gb/s 1 : 2 demultiplexer IC using the 0.1-μm HEMT's [24]. The block diagrams of the MUX and DEMUX IC's are shown in Fig. 7. Both IC's are based on source-coupled FET logic (SCFL) circuitry and employ single-ended input and complementary output interfaces. So, the data and clock input buffer, output buffer, and driver circuit are integrated with the core cells. The SCFL configuration is best suited to InAlAs/InGaAs HEMT's that can provide only normally-on FET's (DFET's). This is because the SCFL circuit is configured with DFET's as well as with EFET's while keeping its high-speed potential.

The core of the MUX has a simple SCFL series-gated selector circuitry with source followers at the output stage (shown in Fig. 8). Internal differential circuitry consists of 20-μm FET's and 130-Ω load resistors. These conditions are the best for minimizing the gate propagation delay while

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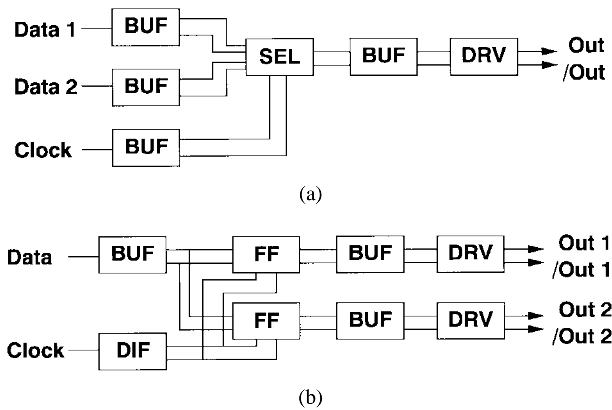


Fig. 7. Block diagrams of (a) MUX and (b) DEMUX IC's.

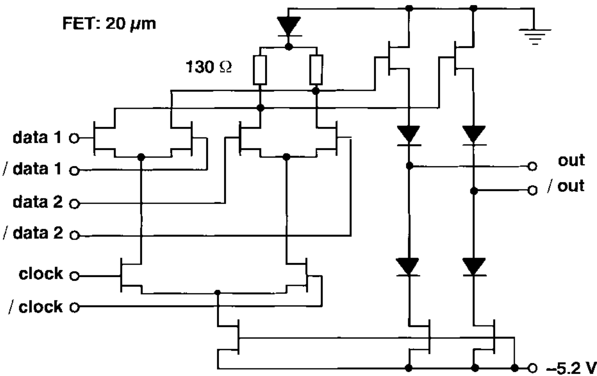


Fig. 8. Core SCFL selector circuit of 2 : 1 MUX.

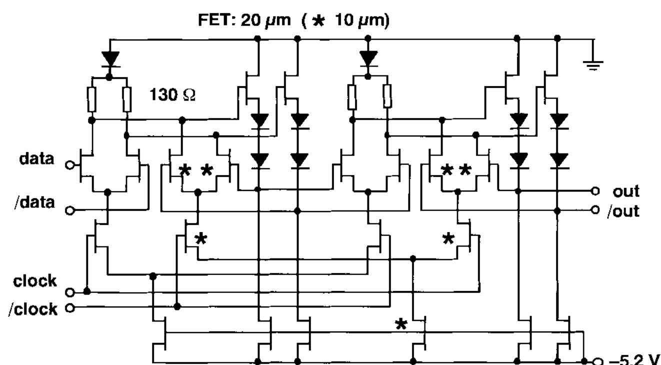


Fig. 9. Core HLO-type D-FF circuit of 1 : 2 DEMUX.

maintaining an SCFL output signal swing. The core of the DEMUX is a high-speed latching operation (HLO)-type D-FF (shown in Fig. 9) [25]. Although the reading circuit of the D-FF consists of 20-μm FET's, the gate width of the latching differential pairs is reduced to 10 μm. This results in 20% higher operation than when using a conventional master–slave D-FF and maintains a wide, quasi-static operation from 1 Gb/s.

Improving the speed of an FF is the key to obtaining faster digital circuits. The trend indicates that the conventional master–slave FF can operate at speeds of one-fifth to one-fourth the transistor f_T for FET devices [26]. This means that a conventional master–slave D-FF needs 200-GHz transistors for 40-Gb/s operation. Even if we adopt an HLO-D-FF, the speed margin is insufficient. To overcome this, we devised a super-dynamic FF circuit that can operate 30% higher than previously-reported FF's [27]. Fig. 10 shows the circuit diagram. The circuit features 1) separation of the current path of the reading and latching circuits, 2) a smaller latching current than the reading current, and 3) a source-coupled negative feedback pair inserted in the latching differential pair. These circuit configurations boost the speed beyond the conventional-design limit because they reduce the load capacitance and effective logic swing without any degradation of the signal transition slew rate. The SD-FF provided a 24-Gb/s decision IC using production-level 0.2-μm gate-length GaAs MESFET's having a f_T of 55 GHz [27].

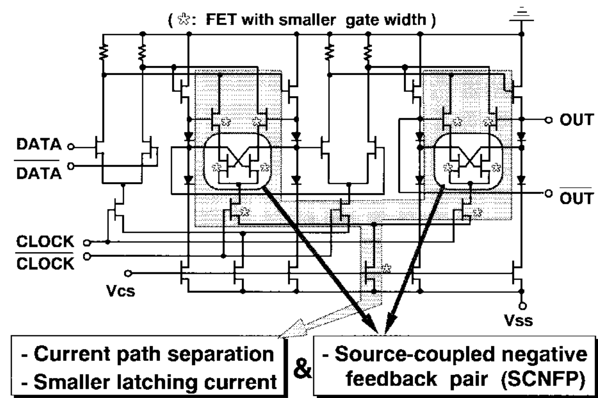
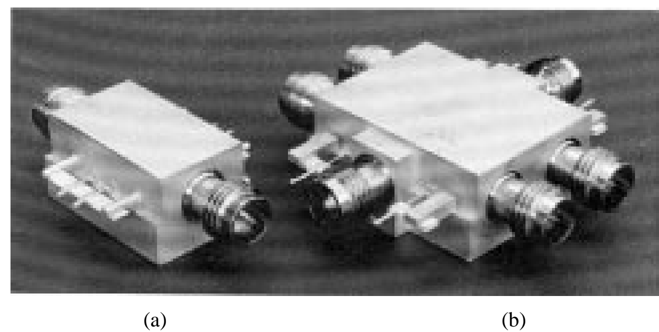


Fig. 10. Circuit diagram of super-dynamic D-FF circuit that can operate 30% faster than previously-reported D-FF's.



(a) (b)

Fig. 11. Appearance of the chip-size-cavity packages for (a) analog IC's and (b) digital IC's.

A super-dynamic decision IC was also fabricated using the 0.1-μm InP HEMT's. The simulated circuit speed exceeded 60 Gb/s. A 40-Gb/s error-free operation was confirmed. The details will be presented in [28].

C. Packaging

Packaging is another key technology for attaining ultra-broadband signal transmission without undesirable losses due to cavity and/or parasitic resonance and coupling. The basic structure we adopted is the so-called "chip-size cavity" package that minimizes the inner cavity [29]. We developed an improved version of the IC packages [30]. Fig. 11 shows the package views, one for (a) analog IC's and one for (b) digital IC's. The RF ports are made with V-band coaxial connectors. The digital-type package can accommodate up to six RF ports. Fig. 12 shows the package structure. A die is mounted on an

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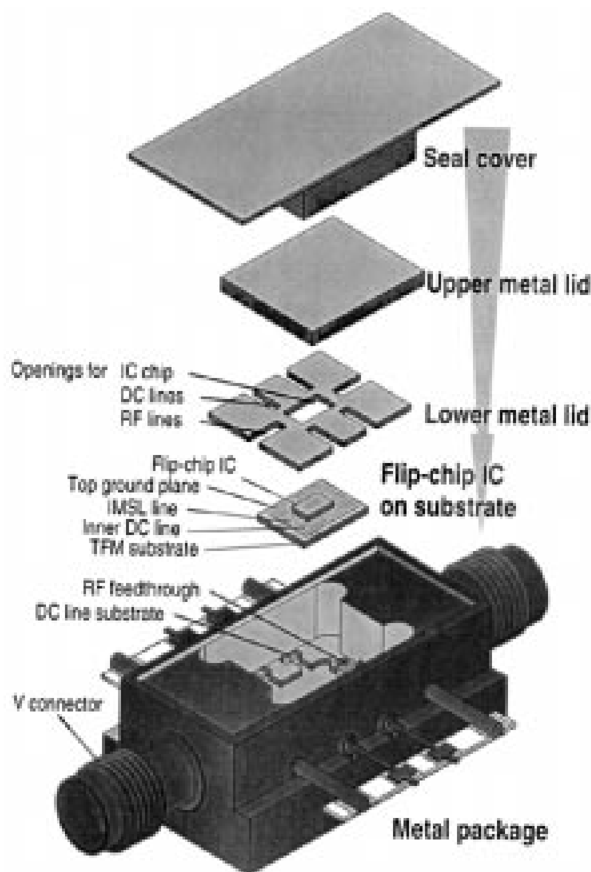

Fig. 12. A view of broadband chip-size cavity package.

inner thin-film multilayer interconnection substrate by means of flip-chip bonding or ribbon bonding. The upper and lower metal lids reduce the size of the inner cavity so as to shift undesirable cavity resonance out of the transmission band. The module with metal lids had a high isolation of more than 60 dB up to 50 GHz. The result agrees well with electromagnetic field analysis [30]. One feature of this module structure is flexibility. If you mount a different type of chip, the design of only the core substrate and the lower lid is subject to change.

The HEMT baseband amplifier was mounted in the analog-type package using ribbon bonding. Both the MUX and DEMUX chips were mounted in the digital-type package using ribbon bonding. The top view of the ribbon-bonded MUX chip is shown in Fig. 13.

V. 40-Gb/s Transmission Experiments

Amplifying, multiplexing, and demultiplexing operations of the packaged IC's were tested at 40-Gb/s and higher. Fig. 14 shows the experimental setup. A complementary pair of fundamental pseudorandom data streams (PN $2^7 - 1$ to $2^{23} - 1$) up to 11.5 Gb/s were generated from a pulse pattern generator (PPG). These were duplexed with appropriate delay against each other by using a GaAs MESFET MUX unit [31] to obtain complementary data streams up to 25 Gb/s, and then input to the MUX module, also with appropriate delay against each other. One MUX output was used as the input of the HEMT amplifier or the DEMUX data input, while

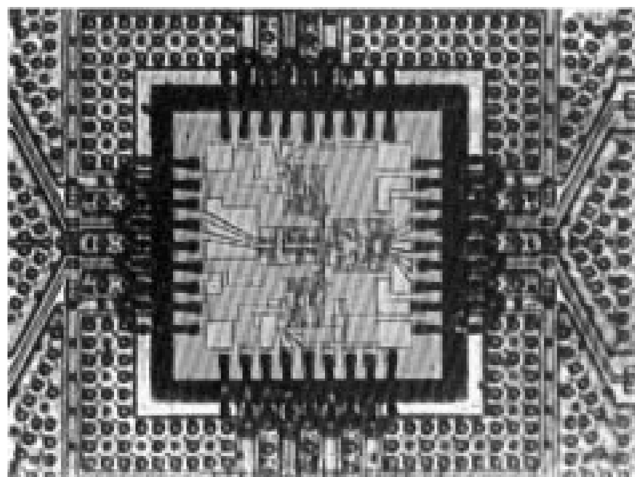

Fig. 13. Top view of the ribbon-bonded MUX chip on a thin-film multilayer substrate.

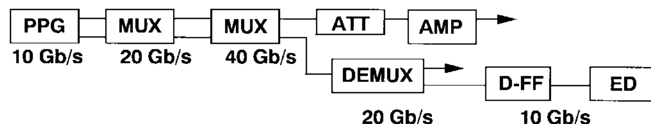

Fig. 14. Experimental set up. PPG: pulse pattern generator; ATT: attenuator; AMP: amplifier; and ED: error detector.

the other was monitored by an HP 54124T digitizing scope. The DEMUX output was again demultiplexed down to the fundamental data rate, and then input to a bit error rate test system. Clock signals for the MUX and the DEMUX were generated by synthesized signal sources whose time bases (10 MHz) were synchronized to the PPG.

The output eye diagrams of the MUX at 40 Gb/s and 46 Gb/s are shown in Fig. 15. There is no waveform deterioration at 40 Gb/s and very clear eye opening was obtained. At 46 Gb/s the output eye is still open. The flat low- and high-level traces demonstrate the flat and broadband performances of the packaging technology.

The output eye diagrams of the amplifier at 40 Gb/s are shown in Fig. 16. When the input data (from the MUX output) was attenuated to 300 mVp-p, an output amplitude of 1200 mVp-p was obtained with a good eye opening.

Fig. 17 shows that when the 40-Gb/s data input from the MUX module was intentionally distorted (equivalent input phase deviation was $\pm 60°$), clear eye opening was obtained from the DEMUX output although the jitter was increased at the fall transition. Under the above conditions, stable MUX and DEMUX operation at 40 Gb/s was obtained and error-free operation was confirmed.

The MUX module was utilized for the first experiment of electrically multiplexed 40-Gb/s $\times$ 4 channel WDM transmission over a 320-km dispersion-shifted fiber [32], and error-free operation with sensitivity degradation of less than 1 dB was successfully achieved. Furthermore, the MUX can directly drive a recently developed MQW electroabsorption optical modulator [33] at bit rates up to 40 Gb/s. The MUX module also verified 40-Gb/s operation of recently developed light source module where a distributed feedback (DFB) laser

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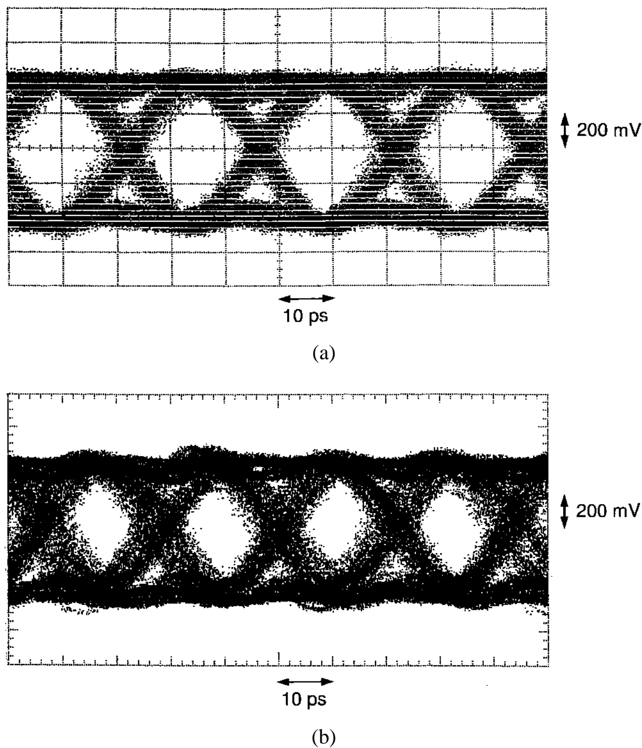

Fig. 15. Output eye patterns of the MUX module at (a) 40 Gb/s and (b) 46 Gb/s.

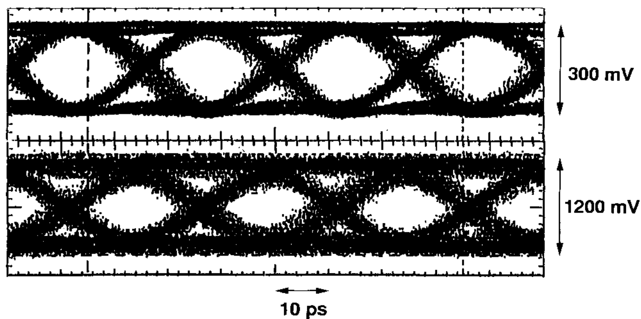

Fig. 16. Output eye patterns of the amplifier module.

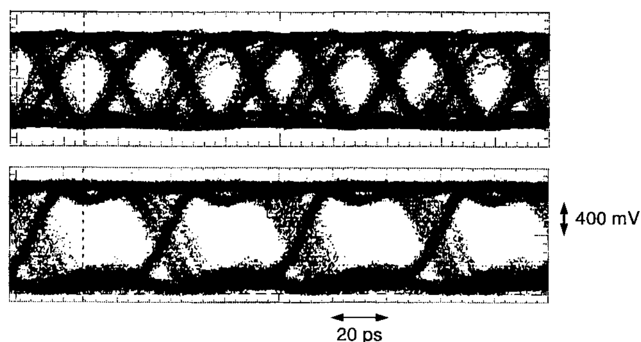

Fig. 17. Output eye patterns of the DEMUX module. Input eye patterns are intentionally degraded to demonstrate the retiming performance of the DEMUX.

and an electroabsorption MQW modulator are monolithically integrated [34]. By using the MUX and DEMUX module, the first experiment of 40-Gb/s fully electrical time-division multiplexed and demultiplexed transmission over 40-km dispersion-shifted fiber was successfully performed [35].

VI. Conclusion

We discussed device, circuit design, and package design technologies applied to future very-high-speed optical communications systems. The synthesis of distributed and lumped circuit design is the key to analog IC's. The digital IC's stay in a relatively lower stage and making full use of analog circuit design in digital IC's is the key to obtaining faster speeds. In fact, introduction of distributed design into digital IC's (especially for sequential circuits such as flip-flops) is really difficult because propagation delay time along with critical signal path limits speed performance. The chip-size cavity structure we developed is quite simple and brought parasitic-free, broadband circuit operation from dc to beyond 50 GHz. Even in the early development stage, the developed IC's and modules show promising performance suited to 40-Gb/s applications. We are now ready to establish fully electrically multiplexed and demultiplexed 40-Gb/s data transmission systems. We are continuing to push toward higher speed operations as well as the further integration of several functional blocks into a single or multichip module. We believe the IC design technology described here will have a great impact on future lightwave communications systems.

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