Multiple-Valued Logic-in-Memory VLSI Based on Ferroelectric Capacitor Storage and Charge Addition

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Abstract

A multiple-valued logic-in-memory VLSI using ferroelectric capacitors is proposed to realize an arithmetic-oriented VLSI with real-time programmable capacitor storage. The use of a remnant-polarization charge on a ferroelectric capacitor makes it possible to perform not only a real-time programmable storage function, but also a linear-sum function, thereby resulting in a compact hardware while maintaining a high-speed processing capability. As a design example, a full adder with a storage capability is evaluated. Its performance is superior to that of a corresponding binary CMOS implementation.

1. Introduction

Dramatic advances in technology scaling give us the capability to realize a giga-scaled system-on-a-chip, while rapid increases in switching speed of logic gates and far slower increases in memory-access speed have led to the communication bottleneck between memory and logic modules in recent deep submicron VLSI[1, 2]. One of the key technologies to solve the above communication-bottleneck problem is to use logic-in-memory VLSI architecture [3, 4]

In logic-in-memory VLSI, storage elements are distributed over a combinational logic-circuit plane, so that highly parallel memory access can be done with small hardware overhead, which makes memory bandwidth large. From this point of view, a logic-in-memory VLSI using floating-gate MOS transistors has been proposed to realize a highly parallel VLSI system [5, 6]. A floating-gate MOS transistor is used as a memory cell device of a flash EEPROM [7]. However, it has been difficult to solve the trade-off between real-time programmability and non-volatility with keeping compactness.

Recently, ferroelectric(FE) memory devices have increasingly attracted attention because they are non-volatile memories as EEPROM with a capability of high-speed read and write operations [8, 9]. Moreover, FE capacitors can be directly sit on top of the transistors by means of stacked vias, hence they have a potential advantage to implement high-density memories. However, very few challenging works about logic-in-memory circuits using FE devices have been reported [10, 11].

In this paper, a new real-time programmable logic-in-memory circuit using FE capacitors is proposed. One of basic components in the proposed logic-in-memory circuit is a 'functional gate' which is used to perform linear summation together with FE capacitor storage. FE capacitors are embedded in the functional gate, so that binary data can be stored as a remnant-polarization charge. Linear summation between stored data in FE capacitors is performed by polarization charge addition. Because the remnant-polarization charge is converted into a corresponding current signal by a capacitive coupling effect, the compact functional gate is realized by using the combination of FE capacitors and an n-channel MOS transistor.

As a design example, a full adder with a real-time programmable storage capability is presented. The transistor counts and the switching delay are reduced to about 70 percent and 54 percent, respectively, in comparison with those of a corresponding binary CMOS implementation under 0.6- m ferroelectric/CMOS.

2. Ferroelectric-based functional gate

2.1. Characteristics of Ferroelectric Capacitors

Figure 1 shows a cross-sectional view and a symbol of an FE capacitor. The FE capacitor is physically distinguished from a regular capacitor by substituting the dielectric with an FE thin film. The FE material consists of a Perovskyte

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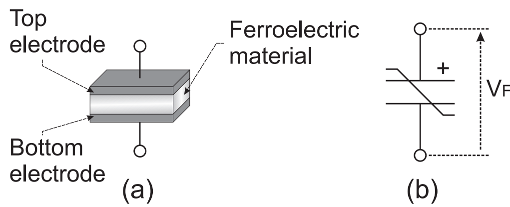

Figure 1. Ferroelectric capacitor. (a) Cross-sectional view and (b) Symbol.

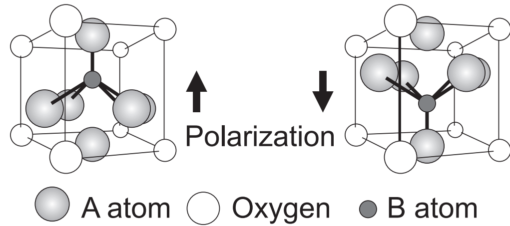

Figure 2. Perovskyte structure.

structure as illustrated in Fig.2, which is transformed when an atom at the center of a lattice causes polarization by a shift from an electrically neutral state according to the external electric field. This polarization causes a hysteresis in the polarization charge versus voltage V plot of the FE capacitor as it is cycled through positive and negative voltage applications as shown in Fig.3. One of the most important characteristics in the FE material is to have a remnant-polarization charge when the voltage V across the FE capacitor is zero, i.e. the FE capacitor is capable of a non-volatile memory device. Figure 3 also shows an example of a binary data assignment with remnant-polarization charges, where the remnant-polarization charge on the FE capacitor is $_r$ for a “0” or -$_r$ for a “1”. As the remnant polarization charge is determined by an applied voltage V, a logic state “0” or “1” can be written into the FE capacitor. Since the transitive speed of polarization states is extremely

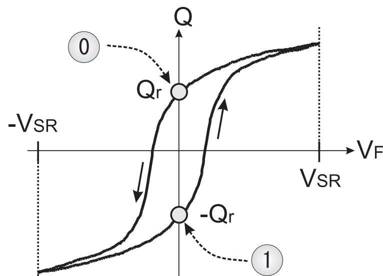

Figure 3. Hysteresis loop characteristic of a ferroelectric capacitor.

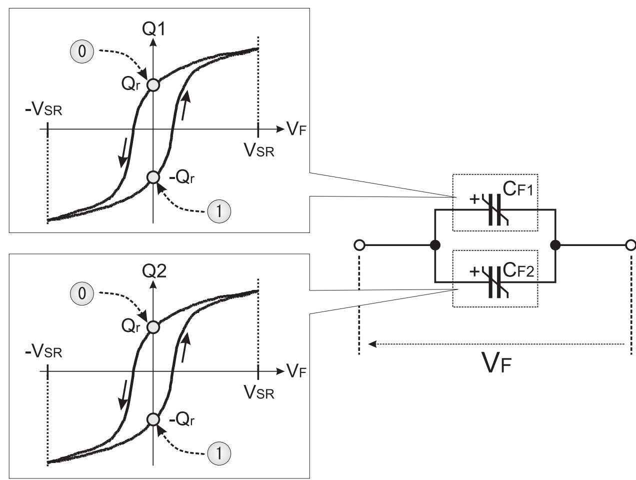

Figure 4. Parallel connection of ferroelectric capacitors.

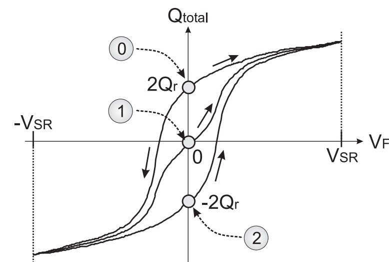

Figure 5. Hysteresis loop characteristic of two parallel-connected ferroelectric capacitors.

high, write speed is as fast as that of DRAM. Consequently, the FE capacitor is capable of a non-volatile and real-time programmable memory device. Recently, several FE capacitors have been reported as memory cells of FE memories (FeRAMs)[12, 13].

2.2. Polarization charge addition using ferroelectric capacitors

If two FE capacitors, $_1$ and $_2$, are connected in parallel as shown in Fig.4, the total polarization charge $_a$ is represented as

$$ {}_a = {}_1 + {}_2, $$

where $_1$ and $_2$ are polarization charges on $_1$ and $_2$, respectively. Figure 5 shows the hysteresis characteristic of the two parallel-connected FE capacitors in case that hysteresis characteristics are represented as shown in Fig.4. If it assumes that a three-valued data is assigned as shown in Fig.5, total remnant-polarization charges, $2\ _r$, 0 and

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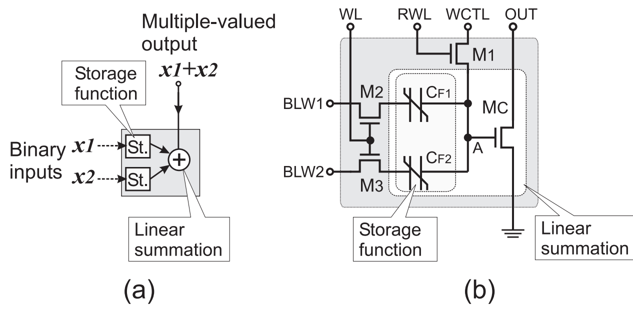

Figure 6. Functional gate. (a) Block diagram and (b) Circuit diagram.

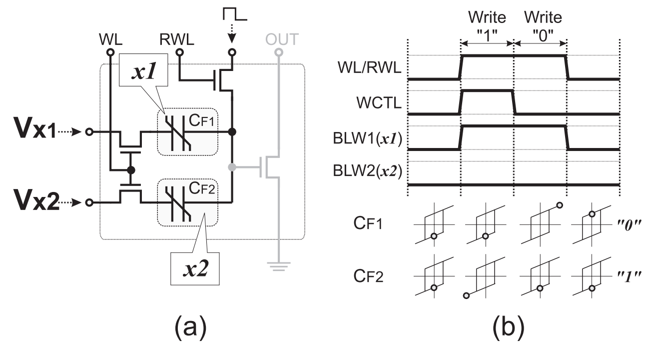

Figure 7. Write operation. (a) Behavior and (b) Timing diagram.

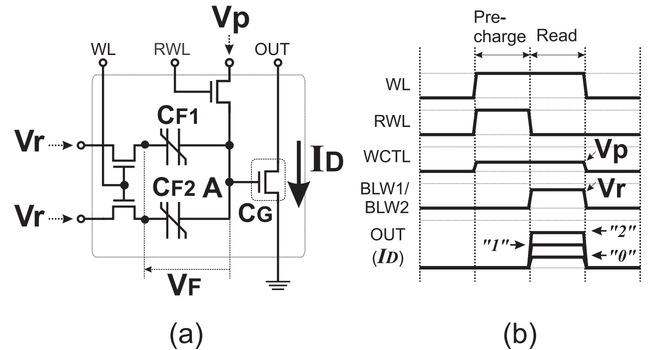

Figure 8. Read operation. (a) Behavior and (b) Timing diagram.

$-2\ _r$, correspond to results of linear summation between binary data stored on $\ _1$ and $\ _2$. For example, let's consider the linear summation in case that binary data stored in $\ _1$ and $\ _2$ are "0" and "1", respectively. In this case, $\ _a$ is indicated as

$$\ _a = \ _r + (-\ _r) = 0,$$

which corresponds to the result of linear summation "1". Consequently, linear summation between stored data is performed by remnant-polarization charge addition with a nonvolatile and real-time programmable storage capability.

2.3. Design of a functional gate using ferroelectric capacitors.

Figure 6(a) shows a block diagram of a functional gate which consists of storage elements and an arithmetic adder. In this module, each of two binary inputs, x_1 and x_2, is stored into storage elements. Then, linear summation $x_1 + x_2$ is performed by an arithmetic adder and a result are converted into a corresponding current signal I . Two binary storage elements and the arithmetic adder are realized by using the parallel-connected FE capacitors described in Section 2.2. The total remnant-polarization charge $\ _a$ is converted into a corresponding multiple-valued current signal by using one n-channel MOS transistor M because $\ _a$ is converted into a corresponding voltage level V on node by capacitive coupling effect thereby generating the drain current I on M . Therefore, the functional gate is designed by using ferroelectric capacitors as shown in Fig.6(b). Three access transistors M_2, M_3 and M are controlled by the word line signal WL and read/write line signal RWL, respectively.

A.Write operation

Figure 7(a) and (b) show basic behavior and the timing diagram in the write operation, respectively. Transistor M_1, M_2 and M_3 are turned on by activating WL and RWL after the two bit lines BLW1 and BLW2 are driven by stored data voltages $V\ _1$ and V (corresponding to x_1 and x_2) , respectively. Then the write control line WCTL is pulsed, that is, pulled up to V_S and subsequently pulled back down to GND. Figure 7 also shows an example of the write operation in case of $x_1 = 0$ and $x_2 = 1$.

B. Read operation

Figure 8(a) and (b) show circuit behavior and the timing diagram in the read operation, respectively. A read operation includes two steps, the precharge scheme and the data read scheme. In the precharge scheme, $\ _1$ and $\ _2$ are precharged to $-V$ by activating RWL and WL after driving WCTL to a precharge voltage V . BLW1 and BLW2 stay the ground level. Figure 9 shows a transition of $\ _a$ in the precharge scheme. Note that V also establishes a charge on as $= V \cdot$.

In the data read scheme, both BLW1 and BLW2 are driven to a read voltage V_r, and RWL is disactivated. This establishes a capacitive coupling consisting of $\ _1 + \ _2$ and . V_r is divided between $\ _1 + \ _2$ and according to their relative capacitance. Depending on $\ _a$, V

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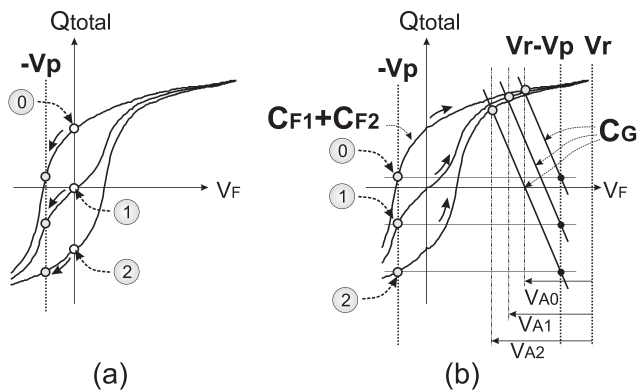
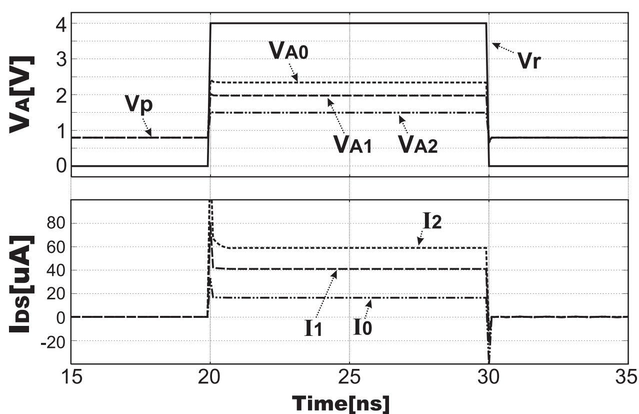


Figure 9. Transition of a polarization charge in the read operation. (a) Precharge phase and (b) Data read phase.



Ferroelectric material	Pb(Zr,Ti)O_3
Remnant polarization charge	28.9 C/cm^2
Coercive voltage	0.90 V
Capacitor area	0.16 m^2

Figure 11. Simulated waveforms.

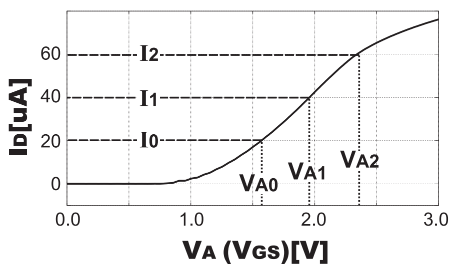


Figure 10. Drain current characteristic of an n-channel MOS transistor M .

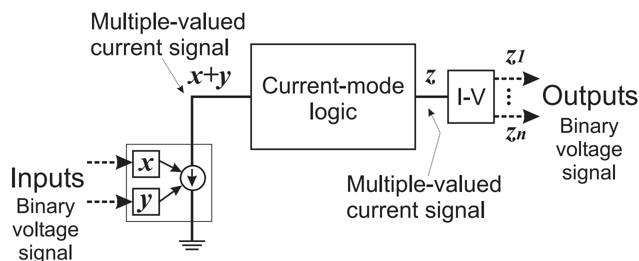


Figure 12. Overall structure of a logic-in-memory circuit.

is represented as

$$(V_r - V\ ) - \quad a = \quad \cdot V - \quad . \qquad (1)$$

Eq.(1) is rewritten as

$$\cdot V \quad = - \quad (V \quad - (V_r - V\ )) + \quad a$$

where $V \ = V_r - V$. Therefore, V can be one of the three values $V\ _0$, $V\ _1$ or $V\ _2$ as shown in Fig.9. Simultaneously, V generates the corresponding drain current I on M as shown in Fig.10. Consequently, the result of linear summation $x_1 + x_2$ is obtained as a multiple-valued current signal. The current level corresponding to $x_1 + x_2$ is determined by V and V_r. Figure 11 shows simulated waveforms in the read operation and characteristics of ferroelectric capacitors under 0.6- m ferroelectric/CMOS.

Consequently, the FE-based functional gate performs voltage-input current-output linear summation with a real-time programmable and non-volatile storage capability.

3. Design of a multiple-valued logic-in-memory VLSI using ferroelectric capacitors

Figure 12 shows a general structure of the proposed multiple-valued logic-in-memory VLSI. Two binary inputs represented as corresponding voltage signals are stored into a functional gate. Then, a result of linear summation is converted into a corresponding current signal. The produced current signal is used in a multiple-valued current-mode (MVCM) logic circuit. The output of the MVCM logic circuit is converted into a binary voltage-signal by using an I-V converter circuit.

3.1. Basic components

Figure 13 shows basic components of the proposed logic-in-memory VLSI.

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	Symbol/Function	Schematic
Functional gate	$x1$ St., $x2$ St., y; $y=x_1+x_2$	Vx1, Vx2, Iy
Wired-sum circuit	$x1$, $x2$, y; $y=x_1+x_2$ (+:Arithmetic sum)	Ix2, Ix1, Iy, Wiring
Comparator	x T y; $y = \begin{cases} 1 & \text{if } x>T \\ 0 & \text{otherwise} \end{cases}$	Ix, Vy, Vref, IT
Differential-pair circuit (DPC)	x, S, x', DPC, y, y'; x x' | y y': 0 1 | 0 S; 1 0 | S 0	Iy, Iy', Vx, Vx', Is
Current mirror	x p x, x	Ix Ix Ix
Current source	K (*K*: Constant value)	Vref, IK
I-V converter	x, x', I-V, y, y'	Vx, Vy, Vx', Vy'

Figure 13. Basic components.

1. *Functional gate:* A functional gate retains two binary data, x_1 and x_2, and generates current output I corresponding to a result of arithmetic summation $x_1 + x_2$.

2. *Wired-sum circuit:* A wired-sum circuit performs arithmetic summation between two inputs current $I_{\ 1}$ and $I_{\ 2}$. Arithmetic summation can be performed by only wiring, which results in compact circuits.

3. *Comparator:* A comparator performs a magnitude comparison between an input current I and a threshold current I , and generates an output voltage V according to a comparison result.

4. *Differential-pair circuit (DPC):* A DPC generates a multiple-valued differential-pair output $(0, S)$ or $(S, 0)$

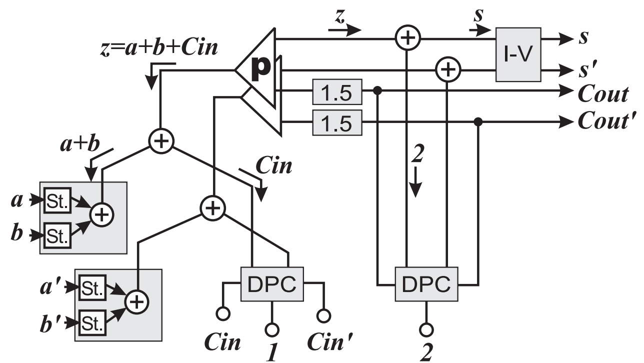

Figure 14. Block diagram of a full adder.

according to a binary differential-pair input, where x' is a complementary signal of x.

5. *Current mirror:* A current mirror produces several replicas of an input current I . The current mirror also has the function of inverting the current direction.

6. *Current source:* A current source is realized by an n-channel MOS transistor with the reference voltage $V_{r\ f}$. The current level is adjusted by the transistor size.

7. *I-V converter:* The function of an I-V converter is similar to DPC with the exception that a binary differential-pair output $(0, 1)$ or $(1, 0)$ is obtained as a corresponding voltage signal. By the combination of the I-V converter and the comparator, it is possible to convert a multiple-valued current signal into binary voltage signals.

3.2. Design example

Figure 14 shows a block diagram of a full adder based on a logic-in-memory circuit which has a real-time programmable storage capability in the combinational-logic circuit plane. A function of the binary full adder is described by arithmetic expressions as

$$\begin{aligned} s &= (a + b + \ _{in}) \quad o \quad 2 \\ &= \quad (a + b + \ _{in})/2 \ , \end{aligned}$$

where $+$ indicates linear summation and $a, b, \ _{in} \in \{0, 1\}$. These equation are rewritten as

$$\begin{aligned} &= \quad a + b + \ _{in} \\ &= \begin{cases} 1 & \text{if} \quad 1.5 \\ 0 & \text{otherwise} \end{cases} \\ s \quad &= \begin{cases} \quad -2 & \text{if} \quad 2 \quad (\quad = 1) \\ & \text{otherwise} \quad (\quad = 0). \end{cases} \end{aligned}$$

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Table 1. Comparison result.

Power supply voltage: 4.0V

	Binary CMOS [1]	Proposed
Transistor counts	40	28
Delay	2.2nsec	1.2nsec
Power dissipation	0.20mW	0.22mW

HSPICE simulation using 0.6-um ferroelectric/CMOS

[1] Binary CMOS full-adder with 6Tr-SRAM cells

In the proposed circuit, linear summation $(a + b)$ between two stored inputs is performed by a functional gate, and the subsequent addition with $_{in}$ is done by only wiring. The final output s is converted into a voltage signal output by an I-V converter. The carry output is a voltage signal output which is produced by a DPC. is directly applied to the DPC of a next full adder without the I-V converter.

3.3. Evaluation

In the proposed circuit, a storage function, a linear-sum function and an output generation are merged into a compact FE-based functional gate. Furthermore, current-mode linear summation between two current signals is realized by just wiring in the MVCM logic circuit. By the combination of voltage and current signals through an FE-based functional gate, a full adder with a real-time programmable storage capability is realized by just 28 MOS transistors and four FE capacitors. Table 1 summarizes the comparison of full adders. Transistor counts, switching delay are reduced to about 70 percent and 54 percent, respectively, in comparison with those of the corresponding binary CMOS implementation.

4 Conclusion

A multiple-valued logic-in-memory VLSI with a real-time programmable storage capability is proposed by using FE capacitors. Polarization charge addition is done by the parallel-connected FE capacitors. Moreover, the remnant-polarization charge is converted into a corresponding current level by capacitive coupling effect, thereby resulting in compact functional gate. A judicious combination of the FE-based functional gate and current-mode logic style makes it possible to distribute real-time programmable storage elements over arithmetic and logic-circuit plane compactly. As a typical example, a full adder with a storage capability is designed, and its execution time and transistor counts are reduced to 70 percent and 54 percent, respectively, in comparison with those of a corresponding to the binary implementation.

The proposed logic-in-memory VLSI based on ferroelectric capacitors offers attractive features for a high-density and highly parallel VLSI system. As a future prospect, it is also important to utilize the logic-in-memory VLSI architecture in the application to fully parallel VLSI processors.

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