# Origin of Positive Charge Generated in Thin SiO<sub>2</sub> Films During High-Field Electrical Stress

Kiyoteru Kobayashi, Akinobu Teramoto, and Hirokazu Miyoshi

Abstract— The characteristics of electron capture in a 131-Å silicon dioxide after hot-hole injection have been studied, which have been compared with those after high-field Fowler–Nordheim (FN) electron injection. After hole injection from the silicon substrate into the oxide, positive charges were accumulated in the oxide and electrons could be captured even at low oxide fields only under the positive gate polarity. The charge centroid of the captured electrons was near the substrate-SiO<sub>2</sub> interface. The low-field electron capture can be explained based on the electron tunneling from the substrate into the positive charge and neutral trap centers created near the substrate-SiO<sub>2</sub> interface.

In order to investigate the initial stage of the oxide degradation due to high-field FN stress, electrons were injected from the gate and the charge fluence was selected to be -1.0 C/cm<sup>2</sup>. After the high-field stress, positive charges appeared in the oxide and electrons were captured only under the positive gate polarity by the positive charge and neutral trap centers, which were distributed near the interface. These facts are explained on the basis of the model describing that hole injection and trapping are the dominant causes for the generation of the positive charge centers during high-field FN stress.

*Index Terms*—Electron tunneling, MOS devices, oxide degradation, trap generation.

#### I. INTRODUCTION

H [GH-FIELD electrical stress to the thin silicon dioxide (SiO<sub>2</sub>) in metal-oxide-semiconductor (MOS) devices causes Fowler–Nordheim (FN) electron tunneling and simultaneously induces various kinds of oxide degradation, such as accumulation of positive and negative charges, trap creation, and interface state generation, eventually leading to catastrophic oxide breakdown. These phenomena are the primary causes limiting MOS device reliability in silicon integrated circuits.

Several studies on the oxide degradation in MOS devices have proposed that holes are produced in the anode of the MOS devices during high-field stress and are injected into the oxide [1]–[7]. Fig. 1 illustrates the schematic energy band diagram that shows the proposed mechanism of hole injection in an MOS structure under negative gate bias. Electrons are first injected from the gate into the conduction band of SiO<sub>2</sub> owing to FN tunneling. Since the electric field is very high, the injected electrons will gain kinetic energy from the oxide

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Fig. 1. Schematic energy-band diagram showing Fowler–Nordheim electron tunneling and hole injection in an MOS structure under negative gate bias.

field and will lose energy by phonon scattering [8]-[10]. The energetic electrons will arrive at the anode (silicon substrate) and will produce electron-hole pairs via the interband impact mechanism [1], [2], [7]. The energy of the electrons entering the anode is converted in part to electron-hole pairs [6]. The holes that are generated with enough energy will be emitted into the valence band of SiO<sub>2</sub> [2], [6]. A small fraction of these holes can be trapped near the  $Si-SiO_2$  interface [2]. In addition, several authors have reported that holes injected into the oxide are captured by defect sites and create positive charge centers [11]–[14], which can capture electrons [11], [12], [14]. It has been also suggested that the hole injection followed by electron injection creates neutral electron trap centers [12], [14]. That is, in the previous studies concerning the oxide degradation during high-field stress and hole injection, it has been proposed that the following four events simultaneously occur during FN electron tunneling:

- 1) the creation of positive charge centers due to hole injection and trapping;
- 2) the electron capture by the positive charge centers;
- 3) the resultant creation of neutral trap centers;
- 4) the electron capture by the neutral trap centers.

However, in spite of extensive research described above, various models, such as migration of hydrogen-related species [15], [16] and electron-emission from neutral traps in the oxide [17], have been proposed to explain the positive charge accumulation and the trap creation during high-field stress. The origin and nature of positive charges and oxide traps

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created during high-field stress are still controversial issues. It is needed to clarify the role of holes in the oxide degradation during high-field stress. In addition, it is important to understand the electrical properties of the positive charges and oxide traps in order to predict their influences on MOS device reliability.

In this article, we first focus on the characteristics of electron capture of the oxide traps generated by hot-hole injection, which are compared with those of the oxide traps created by high-field FN stress. We also demonstrate that hole injection and trapping are the dominant causes for the generation of positive charges and oxide traps during high-field FN stress.

#### II. EXPERIMENTAL

The metal-oxide-semiconductor field-effect transistors (MOSFET's) with p-type source and drain were fabricated on the n-well region in p-type (100) silicon substrates with standard MOS technology. The gate oxide with a thickness of 131 Å was grown using pyrogenic oxidation at 750 °C. A gate electrode was formed from *in situ* phosphorous-doped polysilicon. The thickness of the polysilicon film was 2000 Å and the phosphorous concentration was  $6 \times 10^{20}$  cm<sup>-3</sup>. The source-drain regions were doped with boron ion implantation. After the diffusion and aluminum metallization, all the devices were annealed in a 450 °C hydrogen ambient furnace. The gate oxide thickness ( $t_{cx}$ ) was calculated from the capacitance using the relative dielectric constant of 3.85.

Fig. 2 illustrates a schematic drawing of the biasing conditions in the p-channel MOSFET during substrate hothole injection. The gate electrode was negatively biased with grounded source and drain, and the n-well was positively biased. The electric fields in the gate oxide and the n-well region can be controlled by adjusting the gate bias  $(V_q)$  and the n-well bias  $(V_{\text{well}})$ , respectively. A positive bias  $(V_j)$  was applied to the p<sup>+</sup> diffusion layer to satisfy the forward-bias condition between the p<sup>+</sup> diffusion layer and n-well. Under these conditions, holes are emitted from the p<sup>+</sup> diffusion layer into the n-well and are accelerated toward the gate oxide. A fraction of these holes obtains sufficient energy to overcome the energy barrier of the gate oxide. The energetic holes were injected from the n-well into the gate oxide at a relatively low oxide field (-3.9 MV/cm). A high voltage ( $V_{\text{well}} = 16.5 \text{ V}$ ) was applied to the n-well to have a reasonable hole injection current, which was measured from the gate contact. The number of holes emitted into the gate oxide was counted by integrating the gate current. The dependence of the gate current on the gate area of p-channel MOSFET was checked. The gate current density was independent of the gate area ranging from  $1.0 \times 10^{-6}$  cm<sup>2</sup> to  $1.0 \times 10^{-4}$  cm<sup>2</sup>. Hence it is concluded that holes were injected uniformly over the gate area. In this study, the p-channel MOSFET's with a gate area as large as  $1.0 \times 10^{-4}$  cm<sup>2</sup> were used.

A schematic drawing of the biasing conditions in the p-channel MOSFET during high-field stress is shown in Fig. 3. The n-well, source, and drain were grounded and the gate electrode was negatively biased. The gate current, caused by FN electron tunneling, was maintained at a constant value



Fig. 2. Schematic drawing of the biasing conditions in the p-channel MOS-FET during substrate hot-hole injection.



Fig. 3. Schematic drawing of the biasing conditions in the p-channel MOS-FET during high-field FN stress.



Fig. 4. High-frequency C-V curves for the samples before and after substrate hot-hole injection and then after biasing the gate under the positive or negative gate polarity.

 $(-0.02 \text{ A/cm}^2)$  for 50 s by adjusting the applied gate bias. The oxide field was about -11 MV/cm.

## III. ELECTRON CAPTURE OF THE OXIDE TRAPS CREATED BY SUBSTRATE HOT-HOLE INJECTION

Fig. 4 shows the capacitance–voltage (C-V) curves for the samples before and after substrate hot-hole injection. The C-V curve is shifted toward the negative voltage direction after hole injection. This result is consistent with that hole injection into the oxide creates trapped positive charges [11]–[13].



Fig. 5. Gate current density  $J_g$  at a fixed gate voltage as a function of time for the samples before and after hole injection.

Following hole injection, the gate was subsequently biased under positive or negative gate polarity for 200 s with grounding n-well. During biasing the gate, the gate current was maintained at a constant value (1  $\mu$ A/cm<sup>2</sup>). This current value is selected to be small enough to avoid the creation of additional traps. The C-V curves for the samples after biasing the gate following hole injection are also shown in Fig. 4. We can see that the C-V curve is shifted toward the positive voltage direction under positive gate bias, while the shift is very small under negative gate bias. The shifting of the curve toward the positive voltage direction indicates that electrons are captured in the oxide. The density of electrons captured under negative gate bias is much smaller than that under positive gate bias. The electron capture easily occurs under positive gate bias as compared to negative gate bias.

In order to investigate the electron capture after hole injection, the gate in a p-channel MOSFET was positively biased with grounding n-well and the gate current density  $(J_g)$  at a fixed gate voltage was measured as a function of time. The  $J_g$ -time plots of the samples before and after hole injection are shown in Fig. 5. The level of gate current at the average oxide field of +7 MV/cm is almost constant before hole injection. On the other hand, the current level after hole injection rapidly decays with time and becomes obviously lower than that before hole injection. This low level of current exhibits that electron injection and trapping during biasing the gate produce net negative charges in the oxide. This leads us to claim that the trapped positive charges are neutralized by the electron capture and, in addition, neutral electron trap centers are generated, which can also capture electrons.

Next, in order to investigate the spatial distribution of the captured electrons shown in regard to Figs. 4 and 5, the charge centroid  $\overline{x}_e$  was measured. Following substrate hot-hole injection, the gate was positively biased to inject electrons into the gate oxide. Interrupting the biasing, the gate current-gate voltage  $(I_g - V_g)$  and the drain current-gate voltage  $(I_d - V_g)$  characteristics were measured periodically. The charge centroid  $\overline{x}_e$  of the captured electrons is obtained from the following equation:

$$\overline{x}_e = \frac{|\Delta V_{\rm gn}|}{\Delta V_t + |\Delta V_{\rm gn}|} t_{\rm ox} \tag{1}$$



Fig. 6. Charge centroid of electrons captured under positive gate bias following hole injection.

where  $\Delta V_{\rm gn}$  is the gate voltage shift in the  $I_g - V_g$  curve and  $\Delta V_t$  is the gate voltage shift in the  $I_d - V_g$  curve. The shifts  $\Delta V_{\rm gn}$  and  $\Delta V_t$  were increased with the biasing time even at low oxide fields, such as +2.6 and +7.3 MV/cm. This fact indicates that electrons can be captured at such low oxide fields after hole injection. In Fig. 6, we find that the charge centroids of the captured electrons are located near the substrate-SiO<sub>2</sub> interface and are almost independent of the biasing time. These results show that electron trap centers are distributed near the substrate-SiO<sub>2</sub> interface after hole injection and can capture electrons under positive gate bias.

### IV. MECHANISMS FOR ELECTRON TRANSPORT AND CAPTURE

Mechanisms of the electron capture in the oxide with trapped positive charges are discussed in this section. Fig. 7(a)–(c) illustrates schematic energy band diagrams of the MOS structure with the 131-Å oxide after substrate hot-hole injection. In these figures, a fraction of holes injected into the oxide has been trapped and has created positive charge centers, which are assumed to be distributed near the substrate-SiO<sub>2</sub> interface. In Fig. 7(a), the line A represents the energy barrier of the fresh oxide at the field strength of +5.1 MV/cm. The arrow  $T_1$  indicates an electron tunneling from the conduction band of silicon substrate into the conduction band of SiO<sub>2</sub>. The positive charges located near the substrate-SiO<sub>2</sub> interface induce a deformation of the energy barrier, as shown by the line B. This deformation enhances the tunneling probability of electrons. The current due to the electron tunneling  $T_1$  is increased by the presence of the positive charges.

As shown in Fig. 6, electrons are captured even at low oxide fields under positive gate bias and the charge centroid of the captured electrons is located near the substrate-SiO<sub>2</sub> interface. In order to explain such characteristics of the electron capture, we suggest that electrons are captured due to tunneling from the silicon substrate into the positive charge centers. Fig. 7(a) illustrates three possible tunneling paths of electrons into the states of the positive charge centers. Process (1) is the electron tunneling from the conduction band of silicon, process (2) is tunneling out of the interface state generated by hole injection, and process (3) is tunneling from the top of the valence band of silicon. These processes are referred as the tunneling  $T_2$ . The positive charge centers distributed near the interface could be neutralized due to the tunneling and capture of electrons.



Fig. 7. Schematic energy-band diagrams of the 131-Å oxide under positive and negative gate biases following substrate hot-hole injection. (a) The band diagram at the average oxide field of +5.1 MV/cm showing the electron tunneling into the conduction band of SiO<sub>2</sub> and the electron tunneling into the states of positive charge centers. (b) The neutral trap centers also capture electrons due to the tunneling of electrons from the substrate. (c) The band diagram at the average oxide field of -5.1 MV/cm. The energy barrier for the electron tunneling from the cathode to the positive charge centers is much higher and wider under negative gate bias than under positive gate bias.

The captured electrons can be recombined with trapped holes. This recombination could create different defects, namely, neutral electron trap centers [12]. Since the origin of the neutral trap centers is the recombination between electrons and the trapped holes, it is reasonable to assume that the distribution of the neutral trap centers is identical to that of the positive charge centers. Hence, both the positive charge and the neutral trap centers are assumed to be distributed near the interface. Thus, the neutral trap centers also capture electrons due to the tunneling of electrons from the silicon substrate, as illustrated in Fig. 7(b).

The gate current density  $J_g$  at a fixed gate voltage under the positive gate polarity is given by

$$J_g = J_1 + J_2 \tag{2}$$

where  $J_1$  is the current component due to the electron tunneling  $T_1$  and  $J_2$  is the displacement component due to the electron capture by both the positive charge and the neutral trap centers. As described above, the deformation of the energy barrier due to the positive charges near the interface enhances the tunneling probability of electrons and increases the current component  $J_1$ . The high level of current observed after hole injection in Fig. 5 is due to the increase in the component  $J_1$ and the appearance of the component  $J_2$ .

After a number of electrons are injected into the oxide, the net negative charges appear due to the neutralization of the positive charge centers and the electron capture by the neutral trap centers. After the filling of a large part of these trap centers, the current component  $J_2$  due to the electron



Fig. 8. Variation of the gate voltage as a function of stressing time during high-field FN stress.

tunneling  $T_2$  is substantially reduced, and the oxide barrier is deformed by the net negative charges, as shown by the line C in Fig. 7(b). This deformation reduces the tunneling probabilities of electrons. Therefore, as pointed out in Fig. 5, the current level after hole injection rapidly decays with time and becomes lower than that before hole injection.

As can be seen from Fig. 7(c), the energy barrier for the electron tunneling from the cathode to the positive charge centers is much higher and wider under negative gate bias than under positive gate bias. This large energy barrier results in a small tunneling probability of electrons. Therefore the density of electrons captured under negative gate bias is much smaller than that under positive gate bias, as described with regard to Fig. 4.

# V. ELECTRON CAPTURE OF THE OXIDE TRAPS CREATED BY HIGH-FIELD STRESS

Electron capture of the oxide traps created by high-field stress is studied in this section. For high-field stressing under the negative gate polarity, the gate was negatively biased, as shown in Fig. 2. The FN tunneling current across the gate oxide was maintained at  $-0.02 \text{ A/cm}^2$  by adjusting the applied gate bias. In this article, since we focus on the initial stage of the oxide degradation, the charge fluence was selected to be  $-1.0 \text{ C/cm}^2$ . The variation of the gate voltage  $\Delta V_g$  during the high-field FN stress is shown in Fig. 8. The value of  $\Delta V_g$  was first decreased with time. This decrease is due to positive charge accumulation. After a while,  $\Delta V_g$  was turned to the increase due to electron capture in the oxide. At the charge fluence of  $-1.0 \text{ C/cm}^2$ ,  $\Delta V_g$  was still negative, that is, the positive charges were dominant in the oxide.

Fig. 9 shows the high-frequency C-V curves for the samples before and after the high-field stress under the negative gate polarity. We can see the shifting of C-V curve in the negative voltage direction after the negative high-field stress, which is due to positive charge accumulation in the oxide. Following the negative high-field stress, the gate was positively or negatively biased for 200 s. During biasing the gate, the gate current was maintained at a small value  $(1 \ \mu A/cm^2)$  to avoid the creation of additional traps. The C-V curves for the samples after biasing the gate under the positive or negative gate polarity are also shown in Fig. 9. The C-V curve is obviously shifted toward the positive voltage direction



Fig. 9. High-frequency C-V curves for the samples before and after high-field stress under the negative gate polarity and then after biasing the gate under the positive or negative gate polarity.



Fig. 10. Gate current density  $J_g$  at a fixed gate voltage as a function of time for the samples before and after high-field stress.

under positive gate bias. This result shows that electrons were captured in the oxide. On the other hand, only a small shift toward the negative voltage direction is observed under negative gate bias. This shift indicates that a fraction of electrons, which may be trapped during high-field stress, was detrapped from the oxide. Electron capture easily occurs under positive gate bias following the negative high-field stress, while it is not the dominant phenomenon under negative gate bias.

In order to investigate the electron capture under positive gate bias following the negative high-field stress, the gate current density  $(J_g)$  at a positive gate voltage was measured as a function of time. The  $J_g$ -time plots of the samples before and after the negative high-field stress are shown in Fig. 10. The gate current level at the average oxide field of +7 MV/cm is a constant before the negative high-field stress, while the current level after the stress rapidly decays with time and becomes lower than that before the stress. The low level of current exhibits that electrons were captured and net negative charges were produced in the oxide. The charge centroid  $\overline{x}_e$  of the electrons captured under positive gate bias after the negative high-field stress was shown in Fig. 11. The charge centroids are located near the substrate-SiO<sub>2</sub> interface and are almost independent of the biasing time.



Fig. 11. Charge centroid of electrons captured under positive gate bias following high-field FN stress.

The characteristics of the electron capture after the negative high-field stress shown in this section can be explained by using Figs. 1 and 7(a)–(c). As is described in regard to Fig. 1, electrons injected into the conduction band of SiO<sub>2</sub> owing to FN tunneling will arrive at the anode (silicon substrate) and will produce electron-hole pairs via the interband impact ionization mechanism [1], [2], [7]. The holes generated with enough energy in the anode will be emitted into the valence band of SiO<sub>2</sub>. A small fraction of these holes will be trapped and will create positive charge centers, which are assumed to be distributed near the substrate-SiO<sub>2</sub> interface.

As shown in Fig. 11, the charge centroids of the electrons captured under positive gate bias are located near the substrate-SiO<sub>2</sub> interface and the electron capture occurs even at the low oxide fields, such as +2.6 and 7.3 MV/cm. The electron tunneling from the silicon substrate into the states of trap centers in the oxide band-gap is a possible explanation for these characteristics of the electron capture. As illustrated in Fig. 7(a), the positive charge centers distributed near the interface will be neutralized due to the electron tunneling and capture. The recombination between the captured electrons and the trapped holes could create neutral trap centers [12], which also capture electrons due to the electron tunneling from the substrate, as illustrated in Fig. 7(b). After the filling of a large part of the positive charge and neutral trap centers, the current component due to the electron tunneling  $T_2$  is substantially reduced and net negative charges appear. In addition, the oxide barrier is deformed by the net negative charges, as shown by the line C in Fig. 7(b). This deformation reduces the probability of the electron tunneling  $T_1$ . The gate current due to the electron tunneling  $T_1$  and  $T_2$  is, therefore, decreased with time, as shown in Fig. 10.

As illustrated in Fig. 7(c), the energy barrier for the electron tunneling from the cathode to the positive charge centers is much higher and wider under negative gate bias than under positive gate bias. This large energy barrier results in a small tunneling probability of electrons. Therefore the electron capture easily occurs only under positive gate bias, as is pointed out in Fig. 9.

Thus the behaviors of the oxide charges after high-field stress under the negative gate polarity are successfully explained on the basis of the model describing that the creation of positive charge centers during the high-field stress is due to hole injection and trapping.

#### VI. CONCLUSIONS

The characteristics of electron capture after hot-hole injection into a 131-Å oxide have been studied, which have been compared with those after high-field FN stress.

After hole injection from the silicon substrate into the oxide, positive charges are accumulated and electron capture subsequently occurs even at low oxide fields under the positive gate polarity. After a number of electrons are captured, net negative charges appear. The charge centroid of the captured electrons is located near the substrate-SiO<sub>2</sub> interface. The low-field electron capture is due to the electron tunneling from the substrate into the positive charge and neutral trap centers created near the interface.

After high-field FN stress under the negative gate polarity, positive charges are accumulated in the oxide. In addition, electrons can be captured by positive charge and neutral trap centers which are created near the substrate- $SiO_2$  interface. The characteristics of the electron capture can be explained on the basis of the model describing that hole injection and trapping are the dominant causes for the generation of positive charge centers during high-field FN stress.

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#### REFERENCES

- M. V. Fischetti, Z. A. Weinberg, and J. A. Calise, "The effect of gate metal and SiO<sub>2</sub> thickness on the generation of donor states at the Si-SiO<sub>2</sub> interface," *J. Appl. Phys.*, vol. 57, p. 418, 1985.
- [2] M. V. Fischetti, "Model for the generation of positive charge at the Si-SiO<sub>2</sub> interface based on hot-hole injection from the anode," *Phys. Rev. B*, vol. 31, p. 2099, 1985.
- [3] Z. A. Weinberg, M. V. Fischetti, and Y. Nissan-Cohen, "SiO<sub>2</sub>-induced substrate current and its relation to positive charge in field-effect transistors," *J. Appl. Phys.*, vol. 59, p. 824, 1986.
- [4] C. Chang, C. Hu, and R. W. Brodersen, "Quantum yield of electron impact ionization in silicon," *J. Appl. Phys.*, vol. 57, p. 302, 1985.
  [5] K. F. Schuegraf and C. Hu, "Effects of temperature and defects on
- [5] K. F. Schuegraf and C. Hu, "Effects of temperature and defects on breakdown lifetime of thin SiO<sub>2</sub> at very low voltages," in *Proc. Int. Reliab. Phys. Symp.*, 1994, p. 126.
- [6] K. Kobayashi, A. Teramoto, and M. Hirayama, "Model for the substrate hole current based on thermionic hole emission from the anode during Fowler–Nordheim electron tunneling in n-channel metal-oxidesemiconductor field-effect transistors," J. Appl. Phys., vol. 77, p. 3277, 1995.
- [7] Y. Lu and C. T. Sah, "Two pathways of positive oxide-charge buildup during electron tunneling into silicon dioxide film," *J. Appl. Phys.*, vol. 76, p. 4724, 1994.
- [8] D. J. DiMaria, T. N. Theis, J. R. Kirtley, F. L. Pesavento, D. W. Dong, and S. D. Brorson, "Electron heating in silicon dioxide and off-stoichiometric silicon dioxide films," *J. Appl. Phys.*, vol. 57, p. 1214, 1985.
- [9] M. V. Fischetti, D. J. DiMaria, S. D. Brorson, T. N. Theis, and J. R. Kirtley, "Theory of high-field electron transport in silicon dioxide," *Phys. Rev. B*, vol. 31, p. 8124, 1985.
- [10] D. Arnold, E. Cartier, and D. J. DiMaria, "Acoustic-phonon runaway and impact ionization by hot electrons in silicon dioxide," *Phys. Rev. B*, vol. 45, p. 1477, 1992.
  [11] S. K. Lai, "Interface trap generation in silicon dioxide when electrons
- [11] S. K. Lai, "Interface trap generation in silicon dioxide when electrons are captured by trapped holes," J. Appl. Phys., vol. 54, p. 2540, 1983.
- [12] I. C. Chen, S. Holland, and C. Hu, "Electron-trap generation by recombination of electrons and holes in SiO<sub>2</sub>," *J. Appl. Phys.*, vol. 61, p. 4544, 1987.

- [13] A. V. Schwerin, M. M. Heyns, and W. Weber, "Investigation on the oxide field dependence of hole trapping and interface state generation in SiO<sub>2</sub> layers using homogeneous nonavalanche injection of holes," J. Appl. Phys., vol. 67, p. 7595, 1990.
- [14] K. Kobayashi, A. Teramoto, Y. Matsui, M. Hirayama, A. Yasuoka, and T. Nakamura, "Electron traps and excess current induced by hot-hole injection into thin SiO<sub>2</sub> films," *J. Electrochem. Soc.*, vol. 143, p. 3377, 1996.
- [15] D. A. Buchanan and D. J. Dimaria, "Interface and bulk trap generation in metal-oxide-semiconductor capacitors," *J. Appl. Phys.*, vol. 67, p. 7439, 1990.
- [16] D. A. Buchanan, A. D. Marwick, and D. J. Dimaria, "Hot-electroninduced hydrogen redistribution and defect generation in metal-oxidesemiconductor capacitors," *J. Appl. Phys.*, vol. 76, p. 3595, 1994.
- [17] A. El-Hdiy, G. Salace, A. Meinertzhagen, M. Jourdain, C. Petit, and A. Aassime, "The no-thermal activation of the defect generation mechanism in a MOS structure," *J. Non-Cryst. Solids*, vol. 187, p. 216, 1995.



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