Memory characteristics of metal-oxide-semiconductor capacitor with high density cobalt nanodots floating gate and HfO_2 blocking dielectric

Yanli Pei,[1,a)] Chengkuan Yin,[2] Toshiya Kojima,[3] Masahiko Nishijima,[4] Takafumi Fukushima,[2] Tetsu Tanaka,[2] and Mitsumasa Koyanagi[2]
[1]*International Advanced Research and Education Organization, Tohoku University, 6-6-03 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8578, Japan*
[2]*Department of Bioengineering and Robotics, Tohoku University, 6-6-01 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan*
[3]*Technical Division, School of Engineering, Tohoku University, 6-6-04 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan*
[4]*Institute for Materials Research, Tohoku University, 2-1-1 Katahira, Aoba, Sendai 980-8577, Japan*

(Received 14 May 2009; accepted 7 July 2009; published online 24 July 2009)

In this letter, cobalt nanodots (Co-NDs) had been formed via a self-assembled nanodot deposition. High resolution transmission electron microscopy and x-ray photoelectron spectroscopy analyses clearly show that the high metallic Co-ND is crystallized with small size of ~2 nm and high density of $(4-5)\times10^{12}/cm^2$. The metal-oxide-semiconductor device with high density Co-NDs floating gate and high-*k* HfO_2 blocking dielectric exhibits a wide range memory window (0–12 V) due to the charge trapping into and distrapping from Co-NDs. After 10 years retention, a large memory window of ~1.3 V with a low charge loss of ~47% was extrapolated. The relative longer data retention demonstrates the advantage of Co-NDs for nonvolatile memory application. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3189085]

Memory device structures with metal nanodots floating gate have been considered as a possible solution to scale down nonvolatile memories (NVMs). Compared to semiconductor nanodots,[1,2] metal nanodots with a high work function can provide better data retention due to the formation of a deep quantum well.[3–5] Another advantage is that metal nanodots have higher density of states around Fermi level so that the requirement of high charge storage capacity can be realized. However, some challenges have to be faced, such as the formation of high density nanodots to overcome the electrical fluctuation between memory cells and the prevention of metal oxidation.[6,7] In previous work, we had fabricated tungsten nanodots (W-NDs) with small size and high density by self-assembled nanodot deposition (SAND).[8] However, for the small sized W-NDs, the quantum size effect cannot be neglected, which presumably leads to the degradation of data retention. The metal nanodots with high work function are required to compensate the conduction band upshift caused by quantum size effect. Compared to the tungsten with middle work function (~4.5 eV), the cobalt with high work function of ~5.0 eV is considered as a good candidate.[9,10] In addition, the enthalpy of Co–O bond is 384 kJ/mol, which is much lower than of Si–O (799 kJ/mol), and forming high metallic nanodots in silicon oxide is considered to be easy.[11] In this letter, we have investigated the memory characteristics of high density Co-NDs dispersed in silicon oxide. Here, we employed high dielectric HfO_2 as blocking layer to improve the controllability of gate to write/erase data.

2 in. *p*-type Si wafers with (100) orientation were cleaned with standard Radio Corporation of America (RCA) process, followed by thermal oxidation to form a 5 nm thick tunneling oxide. Subsequently, Co-NDs film with 2 nm thick was deposited onto the tunneling oxide by SAND. In this method, cobalt chips placed on a silicon oxide target were cosputtered in high-vacuum rf sputtering equipment. The size of cobalt chip is in a length of 5 mm, a width of 5 mm, and a thickness of 2.0 mm. To obtain uniform dot size and dot density, the silicon substrate was rotated at a rate of 75 rpm. Subsequently, the postdeposition annealing (PDA) was performed *in situ* at 800 °C for 1 h to improve the quality of Co-ND and silicon oxide matrix. Then, the HfO_2 as thick as 40 nm was sputtered as blocking gate oxide. To prevent the interdiffusion of HfO_2 and Co-NDs, 1 nm thick sputtered SiO_2 was sandwiched between Co-NDs film and HfO_2. The blocking layer was annealed at 600 °C in nitrogen ambient for 30 min. The dielectric constant of HfO_2 was estimated as $\sim20\varepsilon_0$. Finally, in order to fabricate the metal-oxide-semiconductor (MOS) memory device, Al electrode with a diameter of ~0.3 mm was evaporated. As a reference, the MOS capacitor with 2 nm thick sputtered silicon oxide without Co-NDs was fabricated simultaneously. The physical characteristics of Co-NDs were evaluated by high-resolution transmission electron microscopy (HRTEM) and x-ray photoelectron spectroscopy (XPS). The memory properties were measured at room temperature using an Agilent B1500A semiconductor parameter analyzer.

Figure 1(a) shows a cross-sectional HRTEM image of HfO_2/Co-NDs/SiO_2/Si structure. It was clearly observed that the Co-NDs with high density were dispersed in the sputtered silicon oxide matrix. The average size of Co-NDs is about 2 nm. The crystallized Co-ND with obviously visible lattice fringes was evident in Fig. 1(b). To confirm the Co-NDs density exactly, the TEM plane-view image was shown in Fig. 1(c). After PDA, the density of Co-NDs is as high as $(4-5)\times10^{12}/cm^2$.

The chemical composition of Co-NDs film annealed at 800 °C for 1 h is demonstrated by XPS analysis using an Al $K\alpha$ (1486.6 eV) x-ray radiation. To prevent the oxidation of Co-NDs film in atmosphere, 1 nm thick silicon oxide was

a)Electronic mail: peiyanli@sd.mech.tohoku.ac.jp.

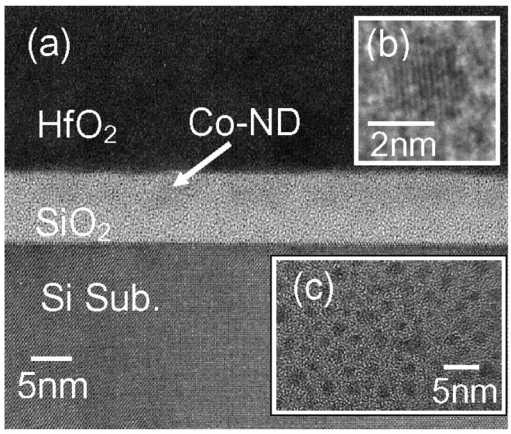

FIG. 1. (a) HRTEM cross-sectional image of HfO_2/Co-NDs/SiO_2/Si structure. (b) An enlarged HRTEM image of Co-ND, (c) HRTEM plane-view of Co-NDs film with 800 °C PDA.

sputtered on 2 nm thick Co-NDs film as cap layer for XPS measurement. Figure 2 shows the Co 2*p* core level XPS spectrum. The peaks at 778.4 and 781.3 eV were obtained by fitting this spectrum. These binding energy values are very close to the values reported for Co–Co and Co–O as references.[12,13] It is worthy to note that the proportion of Co–Co to Co–O bonds is about 2, which was estimated from the XPS spectrum fitting. These results indicate that the Co-ND is a high metallic structure. Some oxidized cobalt is present, which presumably bonds to the silicon oxide matrix. We have reported that W-NDs dispersed in silicon oxide were oxidized seriously.[7] Here, the enthalpy of W–O bond (672 kJ/mol) is close to that of Si–O (799 kJ/mol).[9] In comparison, the enthalpy of Co–O bond (384 kJ/mol) is much lower than that of Si–O.[9] It suggests that the oxygen bonds easier to silicon than to cobalt. Therefore, the high metallic Co-ND was self-assembly dispersed into the silicon oxide matrix.

Figure 3 shows the high-frequency (1 MHz) capacitance-voltage (*C-V*) characteristics with different sweeping gate voltages for MOS capacitor with Co-NDs floating gate and HfO_2 blocking dielectric. The holding time in these measurements is 1 s. Memory windows with counterclockwise hysteresis were observed clearly. The memory window is independent of the measurement frequency (not shown here). In addition, as shown in the insert of Fig. 3, for the reference sample with 2 nm thick sputtered silicon oxide

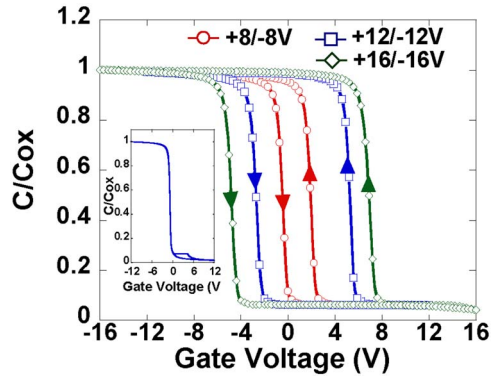

FIG. 3. (Color online) High-frequency *C-V* curves measured at different sweep biases for Co-ND MOS capacitor. The inset is the result of MOS capacitor with 2 nm thick sputtered silicon oxide without Co-NDs.

without Co-NDs, no hysteresis was obtained even at gate voltage sweeping from +12 to −12 V. These results indicate that the memory window is induced by the charge trapping into and distrapping from Co-NDs to silicon substrate. Memory window as a function of sweep gate voltages was summarized in Fig. 4 based on a series of *C-V* measurements. These *C-V* measurements were carried out by applying stress voltages to the gate with holding time of 1 s, followed by bidirectional voltages sweeping. As shown in Fig. 4, the memory window appeared at +5/−5 V sweep gate voltage, and increased with increasing the sweep gate voltage. Finally, it tends to saturation, suggesting that at high electric field region, the current through tunneling oxide to Co-NDs is equivalent with the leakage current from Co-NDs to control gate through blocking oxide. Under low sweep gate voltage of +8/−8 V, a memory window of ~2.45 V was obtained. The maximum memory window of ~12.0 V was observed at sweep gate voltage of +17/−17 V. We had calculated the charge density in Co-NDs by formula as reference.[14] At memory window of 12 V, the trapped charge density was estimated to be $\sim 2.8\times 10^{13}/\mathrm{cm}^2$. Considering the density of Co-NDs, it suggests that one Co-ND can store five or more charges.

Retention characteristics of Co-ND MOS memory capacitor were also investigated at room temperature. Figure 5 shows the data retention characteristics after program/erase (P/E) at ±8 V and ±10 V for 1 s, respectively. As is observed, after ±10 V P/E, the memory window of ~4.5 V remained at retention time of 10^4 s, namely the charge loss of

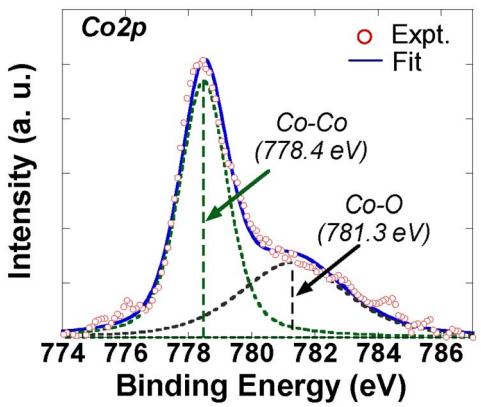

FIG. 2. (Color online) Co 2*p* core level XPS spectrum of Co-NDs film.

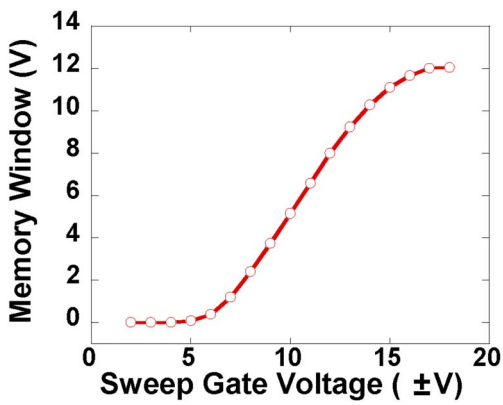

FIG. 4. (Color online) Memory window as a function of sweep gate voltages for Co-ND MOS memory capacitor.

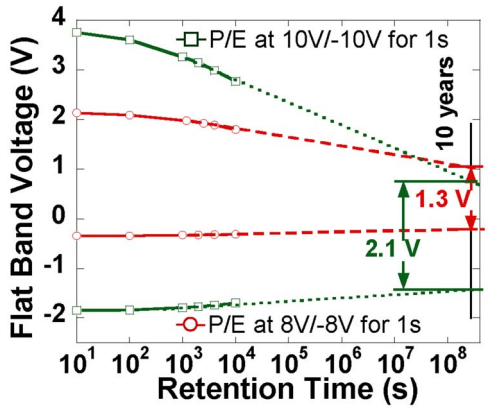

FIG. 5. (Color online) Retention characteristics at zero gate bias and room temperature for Co-ND MOS memory capacitor. The program/erase was done at ±8 and ±10 V for 1 s.

~20%. The logarithmic dependence of the retention characteristics has been observed by various groups.[15,16] Using this extrapolation, a large memory window of 2.1 V and a charge loss of 62% can be estimated after 10 years retention. On the other hand, for the case with lower P/E voltage of ±8 V, the rate of charge loss becomes moderate. At 10^4 s, the memory window of 2.1 V remained with the charge loss of ~15%. After 10 years data retention, a memory window of 1.3 V with a charge loss of 47% was estimated. In previous study, we have reported the retention characteristics of high density W-NDs.[8] In this case, the memory window disappeared at 6×10^7 s.[8] In comparison, relative longer data retention was realized in Co-NDs. It is presumably due to the higher work-function of cobalt.

In conclusion, high metallic Co-NDs dispersed in silicon oxide were formed by SAND method, followed by 800 °C PDA. The high density of $(4-5)\times10^{12}/\mathrm{cm}^2$ and small size of ~2 nm were confirmed by HRTEM. The *C-V* characteristics of MOS capacitor with Co-NDs floating gate and HfO_2 blocking dielectric shows a wide range memory window of 0–12 V. The retention characteristics were also investigated. After 10 years data retention, a memory window of ~1.3 V with a charge loss of ~47% was obtained. The relative longer data retention shows that the Co-NDs with high work function is a good candidate for the next generation NVM application.

This work was partly supported by a Grant-in-Aid for Scientific Research on Priority Area (Grant No. 18063002) from the Ministry of Education, Culture, Sports, Science, and Technology of Japan.

[1] S. Choi, H. Yang, M. Chang, S. Baek, H. Hwang, S. Jeon, J. Kim, and C. Kim, Appl. Phys. Lett. **86**, 251901 (2005).
[2] J. Lu, Z. Zuo, Y. Chen, Y. Shi, L. Pu, and Y. Zheng, Appl. Phys. Lett. **92**, 013105 (2008).
[3] W. R. Chen, T. C. Chang, J. L. Yeh, S. M. Sze, and C. Y. Chang, Appl. Phys. Lett. **92**, 152114 (2008).
[4] S.-S. Yim, M.-S. Lee, K.-S. Kim, and K.-B. Kim, Appl. Phys. Lett. **89**, 093115 (2006).
[5] J. H. Kim, J. Y. Yang, J. S. Lee, and J. P. Hong, Appl. Phys. Lett. **92**, 013512 (2008).
[6] L. Perniola, B. D. Salvo, G. Ghibaudo, A. F. Para, G. Pananakakis, V. Vidal, T. Baron, and S. A. Lombardo, IEEE Trans. Nanotechnol. **2**, 277 (2003).
[7] Y. Pei, T. Fukushima, T. Tanaka, and M. Koyanagi, Jpn. J. Appl. Phys. **47**, 2680 (2008).
[8] Y. Pei, C. Yin, M. Nishijima, T. Kojima, T. Fukushima, T. Tanaka, and M. Koyanagi, Appl. Phys. Lett. **94**, 063108 (2009).
[9] C.-W. Hu, T.-C. Chang, C.-H. Tu, P.-K. Shueh, C.-C. Lin, S. M. Sze, T.-Y. Tseng, and M.-C. Chen, Appl. Phys. Lett. **94**, 102106 (2009).
[10] D. Zhao, Y. Zhu, and J. Liu, Solid-State Electron. **50**, 268 (2006).
[11] D. R. Lide, *CRC Handbook of Chemistry and Physics*, 81st ed. (CRC, Boca Raton, 2000).
[12] I. Alstrup, I. Chorkendorff, R. Candia, B. S. Clausen, and H. Topsoe, J. Catal. **77**, 397 (1982).
[13] B. J. Tan, K. J. Klabunde, and P. M. A. Sherwood, J. Am. Chem. Soc. **113**, 855 (1991).
[14] H. Hanafi, S. Tiwari, and I. Khan, IEEE Trans. Electron Devices **43**, 1553 (1996).
[15] P. Normand, E. Kapetanakis, P. Dimitrakis, and D. Tsoukalas, Appl. Phys. Lett. **83**, 168 (2003).
[16] M.-Y. Hao, H. Hwang, and J. C. Lee, Appl. Phys. Lett. **62**, 1530 (1993).