Integration of Asynchronous and Self-Checking Multiple-Valued Current-Mode Circuits Based on Dual-Rail Differential Logic

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Abstract

A new multiple-valued current-mode (MVCM) integrated circuit based on dual-rail differential logic, whose current-driving capability is high at a low supply voltage, is proposed to realize a totally self-checking circuit and an asynchronous-control circuit. Two nMOS transistors with different threshold voltages are used as complementary pass switches in the proposed differential-pair circuit (DPC), so that the outputs of the DPC always become stable even when non-code-word input $(1,1)$ *are applied, which makes it possible to design a self-checking circuit by using the MVCM circuit. In addition, the dual-rail MVCM circuit technique can be naturally utilized for efficient realization of a two-color dual-rail data-transfer scheme in asynchronous communication. In fact, it is demonstrated that the performance of both a self-checking multiplier and a simple asynchronous control circuit is superior to that of the corresponding ordinary implementation.*

1. Introduction

In the present deep-submicron VLSI era, low-power circuit with keeping a high-speed switching capability at a low supply voltage has been required not only for battery-powered portable applications, but also for reducing the power dissipation of dedicated special-purpose VLSI processors because the extra current density in wires may cause temporal or permanent malfunction due to voltage drops or electromigration [1]-[3]. An MVCM integrated circuit based on dual-rail differential logic has a potential advantage to realize a high-speed logic circuit at a low supply voltage, because the use of a differential-pair circuit (DPC), that is a basic component of the MVCM circuit, makes a voltage swing small yet driving capability large [4]. Moreover, when several DPCs are not active in the MVCM circuit, the gate voltages of current sources in them can be turned off, which makes these power dissipation quite low with keeping a high-speed switching capability [5].

On the other hand, it has been known that data representation based on dual-rail coding is also useful as a code word in self-checking and asynchronous-control circuits. The self-checking circuit, that is one of the important fault-tolerance techniques, has the capability to test for the occurrence of transient and permanent faults within the circuit by a normal input, as well as to detect errors at the input itself [6],[7]. And, an asynchronous-control circuit technique is a key technique to solve a clock-distribution problem due to interconnection complexity in recent deep-submicron VLSI chips [8]-[10]. However, the use of the present binary CMOS gates requires large number of transistors for realizing the above logic circuits based on dual-rail coding.

In this paper, a new MVCM circuit based on dual-rail differential logic is proposed to realize both a totally self-checking circuit and an asynchronous-control circuit with keeping a high current-driving capability at a low supply voltage. A new non-self-checking (NSC) DPC has a redundant function because one of the dual-rail outputs depends on only a single input in the NSC DPC. Accordingly, a self-checking DPC can be designed by the duplication of the proposed NSC DPC. As a result, a self-checking MVCM circuit can be easily designed by using the proposed NSC DPCs in replacement of the original NSC DPC, while other basic components such as comparators and wired-sum circuits still remain used to realize the self-checking circuit.

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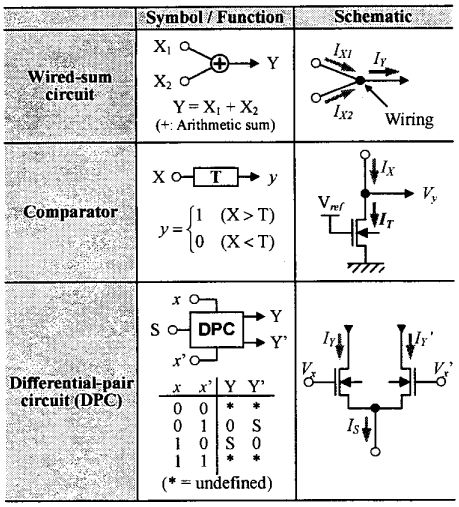

Figure 1. MVCM basic components.

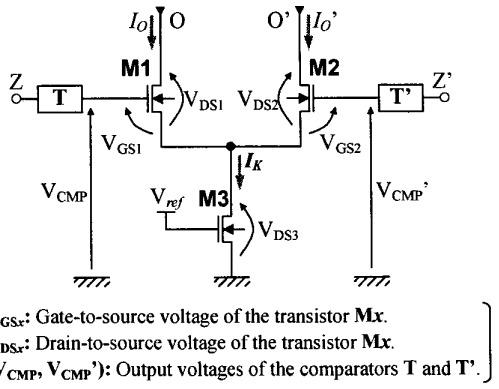

Figure 2. Threshold detector.

As an application, a totally self-checking 8×8-bit multiplier based on radix-2 signed-digit arithmetic [11] is designed by using the proposed NSC DPCs. Its chip area and power dissipation are reduced to 89% and 69%, respectively, in comparison with those of the corresponding fully duplicated implementation under a 0.35-μm CMOS technology.

In the proposed two-color asynchronous communication, a four-valued data value is represented by a pair of seven-valued dual-rail complementary digits. In odd and even phases, the sums of dual-rail digit pairs becomes '3' and '9', respectively. Therefore, the use of this dual-rail coding makes it easy to detect three different states such as an odd-phase data-arrival state, an even-phase data-arrival state and a data-transition state in the two-color asynchronous communication. Moreover, the two-color dual-rail four-valued coding can be easily extended to any multiple-valued data representation. In the viewpoint of compact asynchronous circuit realization, the MVCM circuit technique is suitable because the signal-state detection for asynchronous data transfer is performed by using the sum of dual-rail digit pairs and its threshold operation whose basic operations are compactly realized by using the dual-rail MVCM circuit techniques. As a simple example of two-color asynchronous data transfer, it is demonstrated that the performance of the asynchronous control circuit based on dual-rail MVCM logic is superior to that of the corresponding binary CMOS implementation.

2. Design of a High-Performance MVCM Logic Circuit

Figure 1 shows the basic components of the MVCM logic circuit.

1) *Wired-sum circuit:* In the MVCM logic circuits, arithmetic summation can be performed by wiring without active devices, so that the resulting arithmetic circuits become simple.

2) *Comparator:* A comparator is to compare an input current I_X with a threshold current I_T, and to generate an output voltage V_y.

3) *Differential-pair circuit (DPC):* The function of a DPC is to generate multiple-valued differential-pair outputs $(0, S)$ or $(S, 0)$ in accordance with binary differential-pair inputs as shown in Figure 1.

By the combination of these components, we can design high-performance MVCM circuits. Figure 2 shows a schematic of a threshold detector including two comparators and a DPC. Assume that the output currents of O and O', and the constant current of the current source *M3* are I_O, I'_O and I_K, respectively. When the DPC works correctly, the following condition should be satisfied:

$$I_O(SR) + I'_O(SR) > I_K \quad (1)$$

where $I_O(SR)$ and $I'_O(SR)$ are I_O and I'_O when it is supposed that the transistors *M1* and *M2* operate in the saturation region, respectively. Then *M1* and *M2* operate in the linear region, and I_O and I'_O are described as

$$I_O = \frac{\beta}{2}(2(V_{GS1} - V_T)V_{DS1} - V_{DS1}^2) = f(V_{GS1}), \quad (2)$$

$$I'_O = \frac{\beta}{2}(2(V_{GS2} - V_T)V_{DS2} - V_{DS2}^2) = f(V_{GS2}). \quad (3)$$

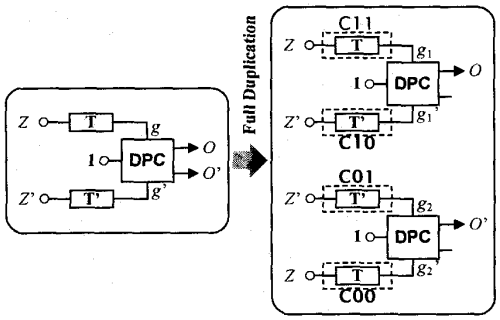

Figure 3. Self-checking circuit by a full duplication.

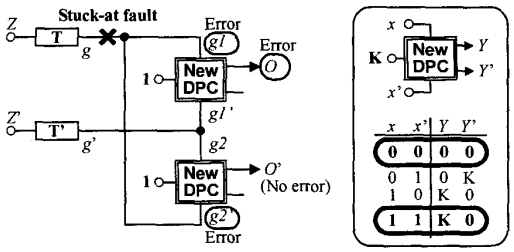

Figure 4. Proposed self-checking circuit and its new DPC function.

where β and V_T are the gain constant and the threshold voltage of transistors, respectively. Since the drain-to-source voltage V_{DS3} of the transistor *M3* is increased so as to satisfy the following condition:

$$I_O + I'_O = I_K. \tag{4}$$

The input voltage swing V_{DPC} of the DPC

$$V_{DPC} = |V_{GS1} - V_{GS2}| \tag{5}$$

must be given by using Eqs. (2) and (3) as

$$|f(V_{GS1}) - f(V_{GS2})| = I_K. \tag{6}$$

In a dual-rail MVCM circuit under a 0.35-μm CMOS technology with a supply voltage of 1.5V, V_{DPC} becomes about 0.3V. Generally, V_{DPC} is so small that a DPC has a high current-driving capability.

3. Applications to a Self-Checking VLSI System

3.1. Definition of a totally self-checking circuit

Self-checking is defined as the ability to verify automatically, whether there is any fault in logic without the need for externally applied test stimuli. We will consider only malfunctions in the circuit caused by a single stuck-at fault. The concept of a totally self-checking circuit, which can generate a detectable erroneous output for every fault from prescribed set during normal operations, is defined as *Fault Secure (FS)* and *Self Testing (ST)*[6].

Let us consider a self-checking design of a threshold detector. First, we define a multiple-valued dual-rail code for detecting errors on multiple-valued circuits. When a pair of R-valued variables (X, X') is a code word, the following equation should be satisfied as

$$X + X' = R - 1. \tag{7}$$

Generally, a duplicated circuit is a totally self-checking circuit. Figure 3 shows a self-checking circuit which has a fully duplicated structure of a threshold detector. Its hardware becomes twice as large as that of the original circuit. This makes the chip area and the power dissipation much larger.

In Figure 3, the functions of two comparators, *C00* and *C01*, are same as two comparators, *C11* and *C10*, respectively. By sharing these comparators, we can get the proposed self-checking circuit as shown in Figure 4. In Figure 4, the number of comparators is half as many as that of Figure 3. However, a single fault makes errors on inputs of two DPCs. To keep self-checking property, the behavior when the input (x, x') is $(0, 0)$ and $(1, 1)$ in the proposed DPC is newly defined as shown in 4. This behavior can be realized by only increasing the threshold voltage of the transistor *M2* in Figure 2. By the definition, the output Y of the DPC is determined by only the single input g.

Now, assume that a single stuck-at fault is occurred on the output g of the comparator T, in Figure 4. This stuck-at fault makes errors on both inputs of two DPCs. However, the error on $g2'$ does not cause an error on the output O' because O' is determined by only a single input $g2$. That is, this circuit has a property of FS. Moreover, when there are no faults in the circuit, dual-rail complementary signals are appeared on inputs of both DPC. Therefore, high current-driving capability is also realized in the proposed circuit.

3.2. Application to a self-checking arithmetic circuit

As a typical application of the proposed MVCM logic circuits, a 8×8-bit multiplier based on radix-2 signed-digit (SD) number addition algorithm is designed and evaluated. SD number representation limits carry-propagation to one

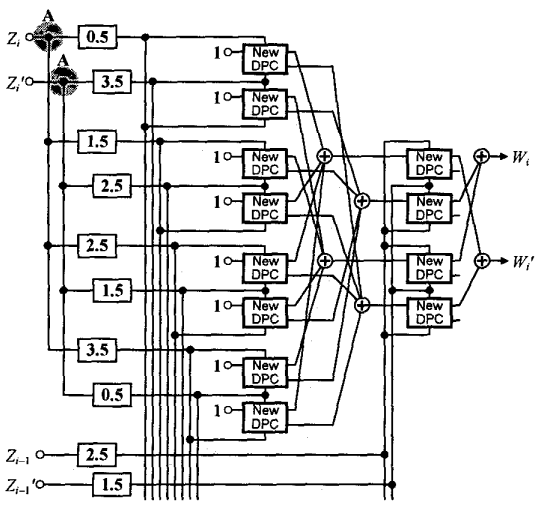

Figure 5. Self-checking intermediate sum circuit.

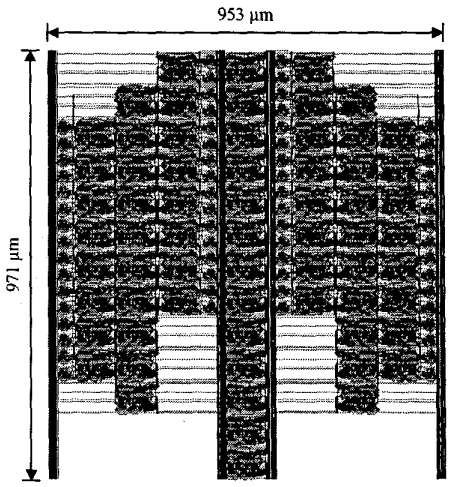

Figure 6. 8x8-bit self-checking multiplier.

digit to the left. Therefore, the addition speed of the SD adder is higher than that of ordinary binary adders [11]. In the dual-rail MVCM logic circuits, addition of each digit can be performed by using the wired sum and SD full adder (SDFA) [4]. Figure 5 shows the intermediate sum circuit of the proposed self-checking SDFA. Using the proposed method, a self-checking SDFA can be designed without duplicating comparators.

Table 1. Comparison of 8×8-bit multipliers.

	Full duplication	Proposed
Supply voltage	1.5 V	1.7 V
Delay	13.2 ns	13.2 ns
Chip area	$1.035mm^2$	$0.925mm^2$
Power dissipation	$38.2mW$	$26.5mW$

Figure 6 shows the 8×8-bit self-checking multiplier using proposed SDFAs. Table 1 summarizes its performance together with those of a full duplicated circuit by HSPICE simulation under a 0.35-μm CMOS technology. In the proposed circuit, the number of comparators becomes half of the full duplicated circuit. As a result, in the multiplier using proposed circuit, the power dissipation can be reduced to 69% as well as the chip area to 89% of a full duplicated circuit.

4. Application to an Asynchronous VLSI System

Figure 7 shows a model of an asynchronous multiple-valued VLSI system. Consider that each module acts like an instantaneous decision element with an unbounded lumped inertial delay in its outputs where the inertial delay physically corresponds to a wire delay. Each module is to be designed using a multiple-valued current-mode logic (MVCM) logic circuit and an associated asynchronous control circuit as shown in Figure 7. In every MVCM logic circuit, each input and output requires a pair of wires containing both the multiple-valued data and the handshaking information, so that we call this "multiple-valued dual-rail" logic. The handshaking information, contained within the wire pairs, disables output changes until the following two conditions are met: (1) the previous output has been used by all logic circuits that receive it, (2) all the new inputs are valid.

In the following section, we discuss about a new multiple-valued dual-rail code which represents the combination of the multiple-valued data and handshaking information, and about the circuit realization which is also suited to the asynchronous system based on the proposed multiple-valued dual-rail coding.

4.1. Two-color dual-rail four-valued coding

In a four-valued dual-rail coding proposed here, the code has four detectable states in both two phases, an odd phase and an even phase. The use of these two different phases makes a spacer negligible in the proposed asynchronous

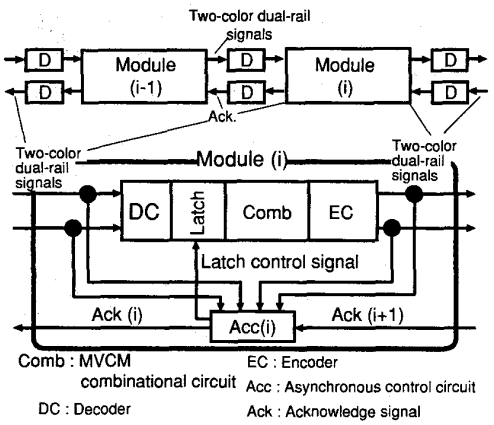

Figure 7. Model of an asynchronous VLSI system.

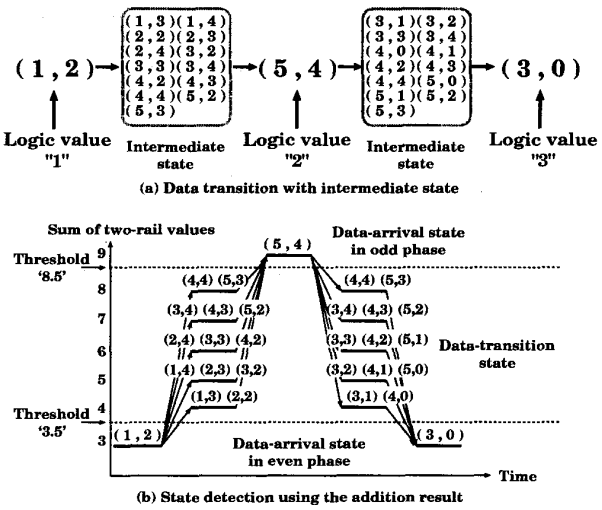

Figure 8. Example of two-color dual-rail asynchronous communication.

system. Data values in each phase are coded by using a pair of two seven-valued digits which are written as follows:

(Odd phase)
$(0,3) \Leftrightarrow$ logic value '0', $(1,2) \Leftrightarrow$ logic value '1',
$(2,1) \Leftrightarrow$ logic value '2', $(3,0) \Leftrightarrow$ logic value '3',
(Even phase)
$(3,6) \Leftrightarrow$ logic value '0', $(4,5) \Leftrightarrow$ logic value '1',
$(5,4) \Leftrightarrow$ logic value '2', $(6,3) \Leftrightarrow$ logic value '3'.

This two-color dual-rail coding is such that the sums of seven-valued digit pairs represented as a data value are always constants three in the odd phase and nine in the even phase, respectively. Therefore, the data transition between an odd-phase data value and an even-phase one is monotonically increased or monotonically decreased, which makes it possible to distinguish data values from transition states in asynchronous communication. The above two-color dual-rail four-valued data representation can be easily extended to any multiple-valued one.

For example, let us consider the two-color four-valued asynchronous data-transfer scheme in case of three sequential input such that logic value '1' in the odd phase, logic value '2' in the even phase and logic value '3' in the odd phase as shown in Figure 8(a). In this scheme, there are several 'intermediate states' between $(1,2)$ and $(5,4)$, and between $(5,4)$ and $(3,0)$. However, note that the result of addition of dual-rail digit pairs distinguishes three different states such that a data arrival state in odd phase, a data arrival state in even phase and a data-transition state, by using two kinds of thresholds, 3.5 and 8.5, as shown in Figure 8(b).

4.2. Design of an asynchronous MVCM logic circuit

Several basic components for multiple-valued asynchronous communication based on two-color dual-rail coding can be compactly realized by using MVCM dual-rail differential logic. A decoder (DC) is a key component that transforms two-color dual-rail signals to one-color ones as shown in Figure 7. In contrast, one-color dual-rail signals are transformed to two-color ones by using an encoder (EC). Figure 9 shows the circuit diagram of a DC and its function. When (x, x') is an odd-phase data value, the control signal ss becomes 1 (that is, both the gate voltages of the nMOS transistors, $M1$ and $M2$, become high), which makes $M1$ and $M2$ turned on. As a result, the dual-rail output signals (y, y') become one-color dual-rail signals. Similarly, an EC can be also designed by using the same circuit of Figure 9. In this way, the use of MVCM logic circuits makes data transformation easily.

The asynchronous control circuit (Acc) shown in Figure 7 receives dual-rail input and output signals of the corresponding module and one-bit acknowledge signal from the next neighbor module, and produces one-bit latch control signal and one-bit acknowledge signal to the previous neighbor module. The signal-state detector (SSD) which detects both odd-phase and even-phase data-arrival states is a key component in the Acc and is easily designed by using the dual-rail MVCM circuit as shown in Figure 10. Since the outputs (V_{st1}, V_{st2}) are binary voltage signals, the resulting one-bit acknowledge signal can be produced by the combination of binary CMOS gates.

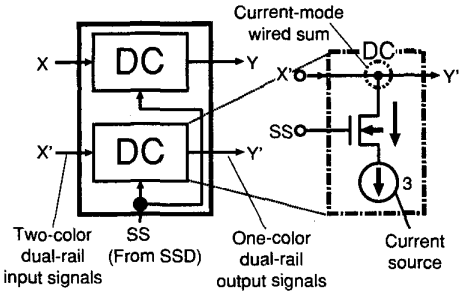

Figure 9. Design of a decoder.

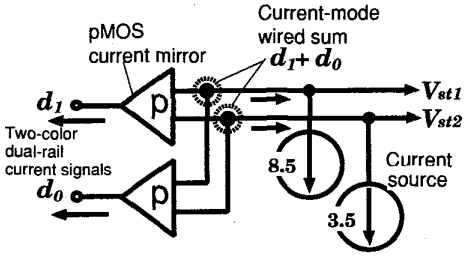

Figure 10. Signal-state detector (SSD).

As a simple example, Table 2 summarizes the comparison of asynchronous control circuits with only a pair of two-color dual-rail input and output signals. In binary CMOS implementation, a two-color dual-rail four-valued data value is represented by four-bit binary signals [12]. A four-valued data value is directly represented by one of four different current levels and a four-valued asynchronous control circuit itself is also compactly designed by using the dual-rail MVCM circuit. As a result, it is demonstrated that the effective chip area and the power dissipation of the asynchronous circuit using the proposed method can be greatly reduced in comparison with those of the corresponding binary CMOS implementation.

5. Conclusion

A new dual-rail MVCM circuit has been proposed to design high-performance self-checking and asynchronous control circuits. The use of both multiple-valued dual-rail data representation and the DPC makes it possible not only to realize a high-speed circuit at a low supply voltage, but also to achieve excellent compatibility with self-checking and asynchronous systems. In fact, the performance of the proposed circuit is superior to that of the corresponding ordinary implementation in terms of the effective chip area, the power dissipation and the switching speed.

Table 2. Comparison of asynchronous control circuits.

	Binary CMOS	Proposed
Area (ratio)	1	0.6
Execution time (ratio)	1	1
Power*1	0.61 mW	0.47 mW

Based on a 0.8um CMOS technology
*1 : Average dynamic power dissipation

As a future problem, it is also important to evaluate the efficiency of the proposed dual-rail MVCM circuit in practical arithmetic VLSI processors.

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