氏名（本籍地）	CHONG WEI SHENG（チョン ウェイ シェン）
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論文審査委員	（主査）東北大学教授 亀山 充隆 東北大学教授 堀口 進　東北大学教授 青木 孝文 東北大学助教授 張山 昌論

論文内容の要旨

1 Introduction

High-performance processors are required for real-time processing in real-world intelligent systems such as intelligent robots and intelligent vehicles. Performance requirements for the processing cannot be achieved using state-of-the-art general purpose processors. Therefore, developments of special purpose processors are important.

The special purpose processors can be realized using application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs). The main problems of ASIC-based realizations are a high cost and a long time-to-market. FPGA-based realizations can overcome the problems because a cost for mask development is not required and realizations based on configurations are possible.

A typical FPGA is based on a cellular array structure. A cell consists of a programmable logic block and a programmable switch block. The logic block is based on lookup tables. The switch block is based on complex crossbar switches and programmable switches. Performance of the FPGA is low compared to that of the ASIC because of the following reasons:

- High power consumption and large area of FPGA switch blocks because there are many power-consuming buffers and configuration memory bits in the switch blocks.
- Large propagation delay between logic blocks because a logic block is connected to another logic block via many slow switch blocks.

To overcome these problems, this research proposes the following reconfigurable VLSI based on fine-grained architectures:

- Low-power field-programmable VLSI (FPVLSI) using a fine-grained VDD-programming scheme.
- High-performance FPVLSI using fine-grained logic blocks.
- Area-efficient multi-context FPGA (MC-FPGA) using fine-grained switch elements.

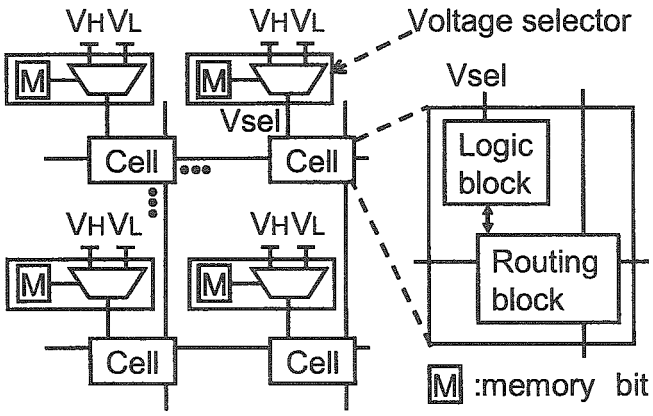

Fig. 1: Architecture of the low-power FPVLSI using multiple supply voltages.

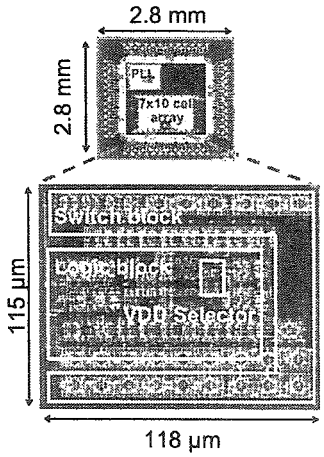

Fig. 2: Layout of the low-power FPVLSI.

2 Low-Power Field-Programmable VLSI Based on A Fine-Grained Supply-Voltage-Programming Scheme

Figure 1 shows an architecture of the low-power FPVLSI. A fine-grained VDD-programming scheme is proposed in the FPVLSI to reduce power consumption under a speed constraint. In the fine-grained VDD-programming scheme, each of the FPVLSI cells has a voltage selector to select a low supply voltage or a high supply voltage. Cells on non-critical paths use a low supply voltage for low power. On the other hand, cells on critical paths use a high supply voltage to meet the speed constraint.

To reduce power consumption of level converters required in a typical VDD-programming scheme, the proposed scheme is level-converter-less by using dynamic-circuit-based logic blocks. In a high-supply-voltage block using low-voltage-swing inputs, level converters are required to prevent direct current in the high-supply-voltage block. Level converters in the typical multiple-supply-voltage scheme cause short circuit current overhead. The power consumption of level converters is significant in field-programmable devices using multiple supply voltages because level converters are required in every cell. Therefore a level-converter-less multiple-supply-voltage scheme is important. The scheme can be realized using CMOS dynamic circuits because there is no direct current in dynamic circuits in ideal cases, regardless of voltage swings of their inputs. The dynamic circuits operate in precharge-evaluation cycles that are controlled by a clock signal. The clock signal switches off a pMOS pull-up transistor and an nMOS pull-down transistor in evaluation and precharge cycles, respectively. Therefore, there is no direct current path from VDD to ground during both precharge and evaluation cycles.

Figure 2 shows a layout of the FPVLSI designed in a 0.18-μm CMOS design rule. For evaluation using ecliptic wave filter, FFT and FIR, power consumption of the proposed FPVLSI is 17% or less compared to that of the static-circuit-based FPVLSI using multiple supply voltages. Power consumption of the proposed FPVLSI is 32% or less compared to that of a dynamic-circuit-based FPVLSI using a single supply voltage.

3 High-Performance Field-Programmable VLSI Based on Fine-Grained Logic Blocks

Complex switch blocks cause low speed performance in the FPGA. Complexity of the switch block can be reduced using a bit-serial architecture because serial data transfer using a single wire leads to a simple switch block. To exploit this advantage, an FPVLSI based on a bit-serial architecture was proposed in a related work. However, coarse-grained logic blocks in the previous FPVLSI have a low utilization. To improve an utilization ratio of the logic block, logic block granularity of the proposed FPVLSI is

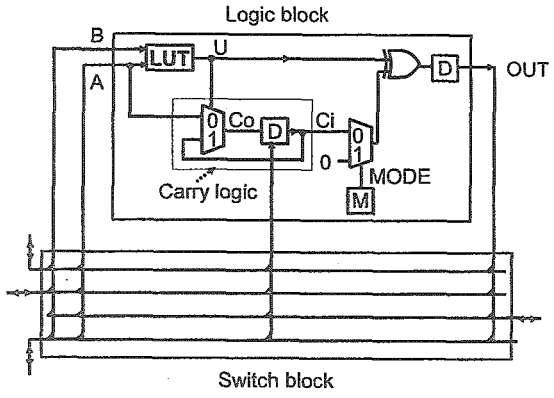

Fig. 3: Detailed structure of a cell in the high-performance FPVLSI.

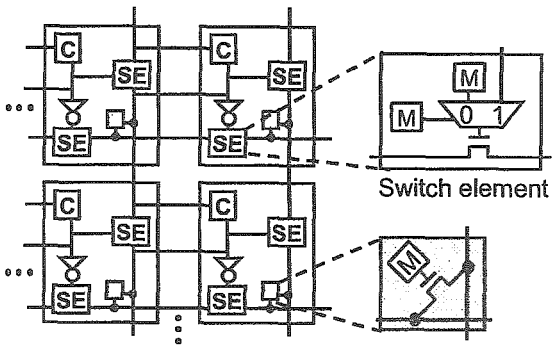

Fig. 4: Switch element block

minimized to use a 2-input 1-output structure.

Since the FPVLSI is targeted for digital signal processing applications, required functions for logic blocks in the FPVLSI are as follow:

- Adder function to be a basic arithmetic operator for arithmetic operations in the digital signal processing applications.
- Arbitrary logic function to achieve flexibility.
- Delay function for storage and timing adjustment in bit-serial operations.

In designing a fine-grained logic block, there are two major concerns as follows:

Functionality: The higher functionality of the logic block requires the larger number of inputs and outputs for the logic block. This increases the complexity of the switch block. On the other hand, the higher functionality of the logic block reduces the number of logic blocks required for implementing a targeted function, and reduces the total delay. Based on this observation, a fine-grained logic block architecture with a functionality of a bit-serial adder is presented. Since a bit-serial adder requires no carry ripple as required in a bit-parallel adder, it can minimize the number of inputs and outputs of the logic block.

Area-efficient implementation: To implement an arithmetic function area-efficiently in the fine-grained logic block, an implementation using LUTs only is not suitable since it requires relatively large LUTs. Two 3-input 1-output LUTs are required, one for a 3-input 1-output sum function, another one for a 3-input 1-output carry function. Therefore, the logic block is implemented based on a hybrid of programmable hardware and a dedicated carry logic. The use of the dedicated carry logic greatly reduces the number of configuration memory bits of the LUT to implement a bit-serial adder.

Based on this observation, the functionalities of the fine-grained logic block are specified as follows.

- 1-bit addition with carry storage
- Arbitrary 2-input 1-output logic function
- Programmable delay

The FPVLSI consists of a mesh-connected cellular array where each cell is connected to only four adjacent cells. A cell has a logic block and a switch block as shown in Fig. 3. The logic block is based on a 2-input LUT and a carry logic. The logic block is programmable for logic, arithmetic and delay mode based on a MODE register. The proposed FPVLSI is compared with typical FPVLSI using coarse-grained 4-input 2-output logic blocks. Under the same area constraints, throughput of an adder tree and a sum of absolute differences using proposed FPVLSI is two times and three times higher than the one using the typical FPVLSI, respectively.

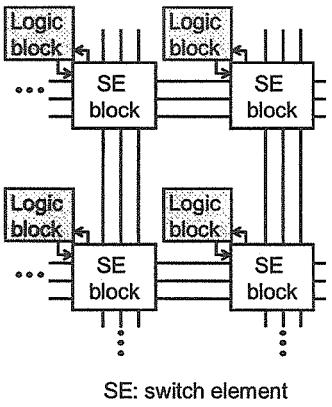

Fig. 5: Basic MC-FPGA architecture using the switch element blocks

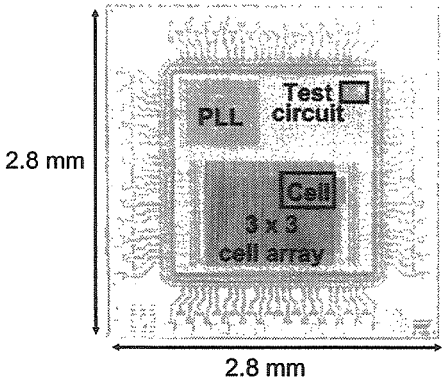

Fig. 6: Micrograph of the MC-FPGA chip

4 Area-Efficient Multi-Context FPGA Based on Fine-Grained Switch Elements

Complex switch blocks reduce area efficiency in the FPGA. The area inefficiency can be improved using a dynamically-reconfigurable VLSI that effectively reuses limited hardware resources in time. One of the popular dynamically-reconfigurable VLSI is a multi-context FPGA (MC-FPGA). The MC-FPGA has multiple memory bits per configuration bit to form configuration planes for fast switching between contexts.

An area of the MC-FPGA is still large compared to the FPGA because the MC-FPGA has a larger number of memory bits, especially in its multi-context switches. To reduce the number of memory bits in the switches, a fine-grained switch element using SRAM memory bits is presented based on the fact that there are redundancy and regularity in configuration bits between different contexts. To achieve compactness and low static power, switch elements using non-volatile functional pass-gates are also presented. The functional pass-gates are based on a ferroelectric capacitor or a floating gate MOS transistor. Figure 4 shows fine-grained switch elements in a switch element block. A single switch element is sufficient to realize switches using configuration bits with a high degree of redundancy. On the other hand, switch element blocks are used to realize switches using configuration bits with a low degree of redundancy.

Figure 5 shows a basic architecture of proposed MC-FPGA consists of adaptive multi-context logic blocks interconnected by the switch element blocks. The main component of the logic blocks is a locally controlled multi-context multi-granularity LUT (MCMG-LUT). The MCMG-LUT is programmable as a 4-input LUT (using four different configuration planes) or a 5-input LUT (using two different configuration planes). Without changing the number of memory bits, the size of an MCMG-LUT can be increased by reducing its number of different configuration planes. The size represents the number of computation data that are selected as inputs of an LUT. An MC-FPGA using a global control signal is not area-efficient because redundant configuration data is stored in the MCMG-LUTs. Each locally controlled MCMG-LUT has a programmable LUT-size controller for efficient mapping without using redundant configuration data. To reduce area overhead of the size-controllers, the switch element blocks are used to form the controllers that are only required if there are different configuration planes.

An 8-context MC-FPGA test chip using SRAM-based switch elements is designed in a 0.18-μm CMOS design rule. A chip micrograph for the test chip is shown in Fig. 6. The test chip is measured and its context switching time is only 3.67ns. A minimum clock period of the test chip is 3.24ns. The proposed MC-FPGAs are compared with a typical MC-FPGA using coarse-grained switches, under the constraint of using 8 contexts. Areas of the proposed MC-FPGAs using switch elements based on SRAM, ferroelectric capacitor and floating gate MOS transistors are 45%, 37% and 5% of the area of the typical MC-FPGA, respectively.

5 Conclusion

Three reconfigurable VLSI based on fine-grained architectures are proposed to improve performance of the FPGA. For future works, low static power architectures and CAD tools for the proposed reconfigurable VLSI should be focused. The static power will be a serious problem in a deep submicron era. The major source of the static power is volatile configuration memory such as SRAM bits. Configuration memory can be realized using non-volatile devices such as ferroelectric capacitors and floating gate MOS to reduce the static power during standby. CAD tools such as a mapping software are important to improve usability of the proposed reconfigurable VLSIs. Supply-voltage-assignment algorithms are important to obtain an optimal VDD-assignment for the proposed VDD-programming scheme. Mapping algorithms for the fine-grained logic blocks are important to increase degree of parallelism in the high-performance FPVLSI. Mapping algorithms that consider redundancy of configuration data are important to exploit features of the proposed MC-FPGA.

論文審査結果の要旨

FPGAに代表されるリコンフィギャラブルVLSIにおいては，プログラマブルな配線や演算セルの稼働率が低く，消費電力が大きいという問題があり，高性能化と低電力化が望まれていた．著者はこのような問題を解決するため，演算機能や電源電圧を細粒度にプログラム可能なアーキテクチャを提案し，その有用性を実証した．本論文はその成果を取りまとめたもので，全文５章よりなる．

第１章は緒言である．

第２章では，処理アルゴリズムを表すデータフローグラフに対してクリティカルパスとなるノードのみに高い電源電圧のセルを割り当てるため，セルごとに異なる電源電圧をプログラム可能な細粒度電源電圧制御方式を提案している．セル間の電圧変換回路のオーバーヘッドを解決するために，電圧変換回路を不要とするダイナミック回路方式に基づくセルを考案し，従来方式と比較して消費電力を一桁程度減少できることを明らかにしている．これはリコンフィギャラブルVLSIの低消費電力化に有用な成果である．

第３章では，算術演算を主体とする応用に適合するリコンフィギャラブル VLSI を提案している．セルの汎用性と小型化を両立させるために，キャリ生成回路，２入力ルックアップテーブル及びレジスタからなるセル構成を与えている．また，ビットシリアルパイプラインアーキテクチャがセル間の相互結合網の複雑さを最小化し，高スループットを達成できることに着目した構成法を与えている．これは算演パイプラインを主体とする画像処理などへの応用に有用であり，従来方式と比較して２倍程度の高速化を達成できることを明らかにしている．

第４章では，複数のコンテクストを動的に切り替え可能な細粒度アーキテクチャを提案している．複数のコンテクストを記憶・選択するためのメモリ・選択回路のトランジスタ数を削減するために，不揮発記憶と演算機能をコンパクトに一体化できる細粒度プログラマブルスイッチエレメントの構成法を考案している．さらに，不揮発記憶の特長を活用すれば小型化と低消費電力化を共に達成できることを明らかにしている．これは実用上重要な成果である．

第５章は，結言である．

以上要するに本論文は，リコンフィギャラブル VLSI の構成要素を細粒度にプログラムすることにより稼働率向上及び低消費電力化を達成する革新的アーキテクチャを開拓し，その有用性を明らかにしたものであり，情報基礎科学の発展に寄与するところが少なくない．よって，本論文は博士(情報科学)の学位論文として合格と認める．