	ふじ わら まこと
氏　　名	藤 原 誠
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指 導 教 員	東北大学教授　小柳　光正
論文審査委員	主査　東北大学教授　小柳　光正　東北大学教授　田中　徹
	東北大学教授　羽根　一博　東北大学教授　桑野　博喜

論 文 内 容 要 旨

Demands for high-speed and high-density data transmission have been increased toward a ubiquitous network society. In telecommunication networks, the transmitting speed has been increasing by improvement of optical interconnection technologies such as a dense wavelength division multiplexing system (DWDM) and an erbium-doped fiber amplifier (EDFA). On the other hand, in short distance electrical interconnections such as board-to-board interconnection and rack-to-rack interconnection, serial transmission lines have been applied instead of parallel transmission lines to realize high-speed and high-density data transmission these days. However, even serial transmission lines are facing their speed barriers due to high-frequency propagation loss, impedance mismatching, jitter, and so on.

On the other hand, large-scale integration (LSI), the performance of LSI chips has been dramatically improved as a result of scaling down the device size. However, the physical limitations such as the thickness of high-k insulator, the length of gate channel, and signal propagation delay are approaching by decreasing device sizes. Therefore, the two or more independent cores are combined into a single die in order to improve the throughput capacity instead of increasing the clock frequency rate of a single microprocessor. It is called " Multi core". In the near future, it is expected to employ a three-dimentional (3-D) LSIs to realize a higher performance and a higher density transmission without scaling-down of divice size because it reduces the wire length in LSI employing a lot of through silicon vias. Furthermore, 3-D LSI has several advantages such as parallel processing, low power consumption, high speed operation, and so on.

However, the transmission speed through electrical chip-to-chip interconnections between conventional LSIs cannot even trail the operating speed of conventional processors. Because the capacitance and inductances of the electrical lines cause many problems such as electromagnetic interference (EMI), cross-talk noise, clock skew and so on. When we employed 3-D LSI having high data transmission speed, these problems become more serious for the electrical chip-to-chip interconnection.

Optical interconnections, instead of electrical interconnections, have been of great interest in high-speed data transfer to overcome these problems.

In this study, all optical interconnect system between chip-to-chip and board-to-board interconnection are proposed to realize prospective demand of higher-speed and higher-density data transmission in the near future.

The all optical interconnect system is composed of new Optical/Electrical PCB (O/E PCB) and "Optical interposer".

New O/E PCB using a polynorbornene (PNB) optical waveguide has three advanced features as follows:

1. Low propagation loss and high Tg using new PNB optical waveguide
2. High flexibility
3. Simple formation process of 45° micromirror by an excimer laser

The O/E PCB can be compatible with standard PCB processes such as photolithography, reflow soldering, and electroplating. The optical waveguide with 45° micromirrors is embedded between flexible PCBs made of polyimide films and Cu circuits.

The production of optical interconnection is facing some technical challenges from the viewpoint of manufacturing. One of the biggest challenges is the alignment between optical waveguides and VCSEL/PD chips. Passive alignment is a promising method for the reduction of the tact time, compared with active alignment using optical instruments such as a laser, a PD, and a stage for precise fiber positioning. Another problem is the difficulty in integrating VCSEL/PD chips on an LSI chip or an interposer because VCSEL as a representative GaAs compound device is not compatible with Si devices such as complementary metal oxide semiconductor (CMOS). Many modules integrated with VCSEL/PD chips on a Si substrate have been developed for chip-to-chip optical interconnections. However, these optical interconnections have a long coupling distance between VCSEL/PD chips and the waveguide. Therefore, a microlens was employed to reduce their coupling loss. A number of research groups have developed new optical components to reduce the coupling loss, such as microlens, optical connection rod, polymer pillars, and optical pin. However, complicated processes are required for the fabrication of their components.

To overcome these problems, we propose a new optical interposer using a passive alignment technique, in which we formed chip-size through-Si holes on Si wafer used as an interposer substrate and embedded VCSEL/PD chips into the chip-sized holes. New optical interposer has 4 advanced features as follows:

1. Through-Si via (TSV) connection between LSI chips and VCSEL/PD chips
2. Self-alignment of VCSEL/PD chips
3. Short optical distance between PNB optical waveguide and VCSEL/PD chips
4. Low optical loss with PNB optical waveguide

New optical interposer consists of PNB optical waveguides with 45° micromirrors and recessed VCSEL/PD chips into a Si substrate having chip-sized through-Si holes. 3-D LSI chips with processor elements are connected to each other by optical interconnections. PNB optical waveguides are formed on the rear surface of the Si substrate. VCSEL/PD chips are buried in the through-Si holes formed by deep reactive ion etching (RIE) in the Si substrate and electrically contacted with solder bumps to metal wirings connected to 3-D LSIs through vertical interconnections. Electrical signal output from a 3-D LSI is converted into optical signal via a VCSEL chip. The optical signal is reflected by a 45° micromirror and transferred to a PD chip through an optical waveguide. Then, the optical signal is converted into an electrical signal again, and finally transmitted to another 3-D LSI.

First, TSVs are short electrical lines to prevent from degrading the signal properties and delaying in transmission of signals.

Big advantage of this optical interposer is that a large number of chips can be aligned passively and bonded simultaneously. All VCSEL/PD chips are moved to the designated position using the surface tension of a molten solder upon heating after the chips are recessed into the holes formed all over the Si substrate.

Other advantages of this optical interposer include low coupling and propagation losses. VCSEL/PD chips are located at the closest point to the optical waveguide. Therefore, the gap between the optical waveguide and VCSEL/PD chips can be minimized. In addition, the low coupling loss is derived from the high-precision passive chip alignment assisted using chip-sized through-Si holes and surface tension of a molten solder. The use of the PNB optical waveguide can achieve the low propagation in this optical interposer.

Eventually, integration of both new technologies, O/E PCB and Optical interposer, realizes the all optical interconnect system.

In this system, new polymer optical waveguide has to apply to achieve a lot of feature as described later. In general, polymer optical waveguides have potential disadvantages in their thermal properties or transparency. A high-heat resistance of more than 250 °C is an indispensable property required to endure a reflow soldering process in the bonding of the electronic/optical components on PCBs. Another important property involves high transparency at around 850 nm because VCSELs, which are widely used for high-speed and short-distance optical interconnections in a gigabit ethernet, can emit an 850 nm light.

Fluorinated polyimides are well known to be high heat resistant polymers for optical waveguides. However, waveguide formation using the polyimides requires complicated and high-temperature processes such as RIE and curing for imidization. In addition, sidewall roughness caused by the RIE process produces scattering loss. Acrylate polymers are representative of highly transparent polymers and have been applied to polymeric waveguide materials. Furthermore, acrylate polymers are formed by low-cost fabrication processes such as photolithography and embossing methods. However, acrylate polymers are thermally unstable at temperatures above 150 °C. Eventually, conventional polymer optical waveguides only nominally integrate with PCBs. However, our newly developed waveguides can easily overcome these problems. We developed new PNB optical waveguides with a low optical loss of 0.029 dB/cm at a wavelength of 830 nm and with high heat resistance (T_g = 270 °C) by a simple fabrication process without RIE, wet etching, and developing. And the transmission of 10 Gbps-data rate was confirmed by the eye pattern measurement.

The O/E PCB described above was fabricated as follows: The PNB optical waveguide was formed between the flexible PCBs. The flexible PCBs composed of a polyimide film and a Cu foil, were drilled to form through holes. Then, the flexible PCBs with the optical waveguide was plated with copper to fill the through holes by the standard plating processes. Third, the electric circuits were patterned on the flexible PCBs by photolithographic and etching processes. Next, it was put between other flexible PCBs using a pressing machine. Finally, the 45° micromirror was formed through the windows of flexible PCBs by excimer laser processing.

The PNB waveguide can withstand PCB fabrication processes such as plating, photolithography, Cu etching, and pressing. The O/E PCB was fabricated successfully for a cellular phone application with flexible parts. 45° micromirrors with a low loss of 0.7 dB were also successfully formed.

In optical interposer, tapered via formation is necessary for the subsequent conformal deposition of barrier and metal seed layers. The vias with a straight sidewall fabricated by deep RIE make it difficult to uniformly deposit the layers on the bottom and sidewall of the resulting vias by sputtering. In addition, the following copper electroplating process results in trapped voids inside the vias with the straight sidewall. In this work, our tapered vias are fabricated by a novel two-step etching process consisting of the Bosch process and isotropic etching. First, silicon dioxide (SiO_2) of 600-nm thickness was formed on a Si substrate by thermal oxidation. Then, the SiO_2 was excessively etched by buffered HF after photolithographically pattering of TSVs. After that, the Si was etched to form deep holes by the Bosch process, and then, the Si was isotropically etched with SF_6, O_2, and C_4F_8 gases. The subsequent thermal oxidation provides conformal deposition of a 600-nm-thick SiO_2 layer on the resulting Si vias. Ta as a barrier layer and Cu as a seed layer were sequentially deposited by sputtering on the SiO_2 layer, followed by Cu electroplating for via filling. After the electroplating, Excess Ta and Cu layers on the surface of the Si substrate were removed by a mechanical polishing process and a wet etching process. After that, electrical circuits were patterned on the surface of the substrate. The backside of the Si substrate was grinded until the thickness of the substrate decreases to 150 μm. Finally, electrical circuits were patterned again on the backside of the thinned substrate. The via after etching by the Bosch process has 163 μm in depth and 32 μm in top size and bottom sizes, whereas the via after isotropically etching has 168 μm in depth, 64 μm in top size, and 34 μm in bottom size. The taper angle of 82° was obtained by the second isotropic etching step. By changing the etching time on the first Bosch process and the second isotropic etching, the depth of TSVs and the degree of taper can be well controlled. Ta and Cu layers were turn out to be uniformly formed on the tapered via surface by sputtering. The resulting tapered TSVs were completely filled with Cu. The average of resistance per a formed taped TSV was 84 mΩ.

The pattern size of through-Si holes for embedding VCSEL/PD chips was designed to be 30 μm larger than that of VCSEL/PD chips. The depth of the holes formed all over the Si substrate can be kept constant at 150 μm. The sidewall of the through-Si hole was formed without tapered profile. In addition, VCSEL/PD chips can be self-assembled onto the predetermined bonding area using a surface-tension-driven restoring force from a molten solder upon heating. Therefore, high-precision alignment can be realized without a large coupling error resulting from chip shifting, inclining, and rotation. As a result, the variation in the mounting place of VCSEL/PD chips was within 10μm. The variation value was enough to align to multimode optical alignment. Therefore, very simple and unique passive alignment method was developed. This method overcame the alignment problem of optical interconnection.

The embedded VCSEL chip in the optical interposer made sure to operate through tapered TSVs and electrical pads with solder. A light signal emitted from the VCSEL chip buried in the chip-size cavity was clearly observed. The I-V curve of the VCSEL through tapered TSVs was measured and the characteristic of the VCSEL electrically connected through the TSVs was almost the same as that of a primary VCSEL chip. This result indicates that the optical interposer can perform as a high quality optical interface of 3-D LSI.

Next, the relationship between mirror coupling loss and coupling distance was evaluated to estimate the coupling loss of the optical interposer. The coupling distance between the VCSEL/PD chips and waveguide in the fabricated optical interposer is less than 50 μm. Thus, the mirror coupling loss of this optical interposer is found to be less than 1.0 dB.

The PNB optical waveguides with 45° micromirrors were fabricated on the interposer. The thickness of under cladding layer, core layer, and upper cladding layer was 5, 35, 5 μm, respectively. The loss of the PNB optical waveguide was 0.07 dB/cm. The angles of formed the micromirrors were 44.5°. All the components of the optical interposer was formed and integrated, and the ICs were mounted on the optical interposer.

As described above, in this study, new PNB optical waveguide was developed. And also, the O/E PCB with flexible part was successfully fabricated using new PNB optical waveguide. In addition, the optical interposer was successfully fabricated. Besides, very simple and unique passive alignment method was developed and resolved alignment problem of optical interconnection. Therefore, the all optical interconnect system between chip-to-chip and board-to-board interconnection are fundamentally constructed.

論文審査結果の要旨

高度情報社会の実現を目指して，高速データ転送に対する要求が益々高まっている。これまで，コア系やメトロ系，アクセス系などの大規模な通信ネットワークには光ファイバーが用いられて，高速のデータ転送が行われてきた。一方，ネットワークを構成する通信機器や情報機器内部では，相変わらず，電気配線によるデータ転送が主要な手段として用いられている。しかし，ユビキタス社会へ向けて，情報のデジタル化が急速に進む中で，通信ネットワークだけでなく，コンピュータや複写機などの情報機器や家電機器，自動車用電子機器などにおいても，光による高速データ転送を取り入れようとする動きが活発になってきている。本論文は，これらの機器に装填されるボード（配線基板）内においても，光による高速データ転送を可能とするために，その鍵となる光インターコネクション技術ついて研究したもので，全編6章よりなる。

第1章は緒論であり，本研究の背景と目的を述べている。

第2章では，これまで報告されている光電気複合基板の性能比較を行い，それらの結果に基づいて新しい光電気複合基板とそれを用いた超高速光インターコネクションシステムの提案を行っている。これは，有用な成果である。

第3章では，本研究で提案した光電気複合基板の重要な構成要素である光導波路を，ポリマー材料であるポリノルボルネン（PNB）を用いて作製し，0.029dB/cm（測定波長：830nm）という極めて小さな光信号伝達損失を実現している。また，実際に光による信号伝達特性を評価し，10Gbpsという高速のデータ転送に成功している。これらは，重要な成果である。

第4章では，ポリノルボルネン（PNB）光導波路とリジッド/フレキシブル基板を複合化することによって，光電気複合リジッド/フレキシブル基板の作製に成功している。発光・受光素子と結合する部分の光導波路に，エキシマレーザーを用いて微小な45°ミラーを形成し，光導波路を伝播してきた光信号を直角に折り曲げることができることを確認している。ミラーによる伝播損失として0.78dBという良好な値を得ている。これらは，重要な成果である。

第5章では，本研究で提案したチップ間光インターコネクション用光インターポーザーの詳細構造について検討するとともに，光インターポーザーを実現するための各要素技術，1)光インターポーザー基板に発光・受光素子を埋め込むためのキャビティ作製技術，2)キャビティ内に高精度で発光・受光素子を埋め込むための一括セルフアラインメント技術，3)発光・受光素子からの端子取り出しのためのシリコン基板貫通ビア（Through Si Via: TSV）技術を確立している。これらの技術を用いて光インターポーザーを作製し，搭載した発光・受光素子が良好に動作することを確認している。また，45°ミラーを介した発光・受光素子と光導波路の間の光結合損失として1dB以下という非常に低い値を得ている。これらは極めて重要な成果である。

第6章は結論である。

以上要するに本論文は，ポリノルボルネン（PNB）光導波路と，発光・受光素子を埋め込んだ光インターポーザーを搭載した光電気複合リジッド/フレキシブル基板を作製し，ボード内およびLSIチップ間で高速の光データ転送が可能であることを実証したものであり，バイオロボティクスおよび半導体工学の発展に寄与するところが少なくない。

よって，本論文は博士(工学)の学位論文として合格と認める。